

# Compal Confidential

Model Name : A4DBH

File Name : LA-B731P

BOM P/N:43

ZZZ1  
LA-B731P  
DA40008X000  
DA2@

ZZZ2  
LS-A131P  
DA4001PG010  
DA2@

ZZZ3  
LS-B733P  
DA60018L000  
DA2@

ZZZ4  
LS-A133P  
DA600101010  
DA2@

ZZZ5  
LS-A134P  
DA4001PH010  
DA2@

ZZZ6  
LS-B734P  
DA6001B8000  
DA2@

ZZZ7  
HDMI LOGO  
RC0000003HM  
HDMI@

ZZZ8  
LS-B732P  
DA4001YF00S  
DA2@

ZZZ11  
PCB  
DAZ18000300  
DAZ@

# Compal Confidential

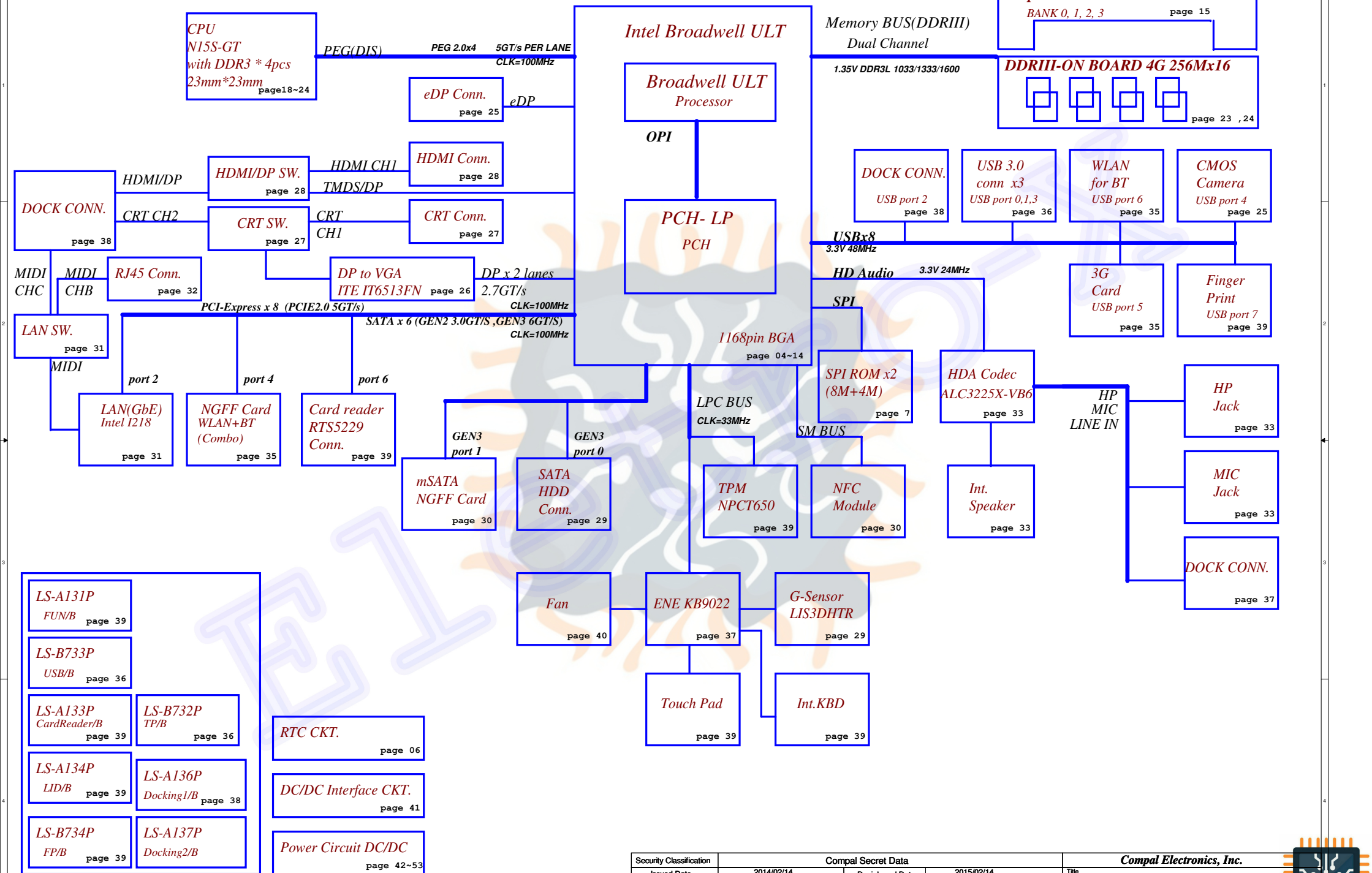
## A4DBH M/B Schematics Document

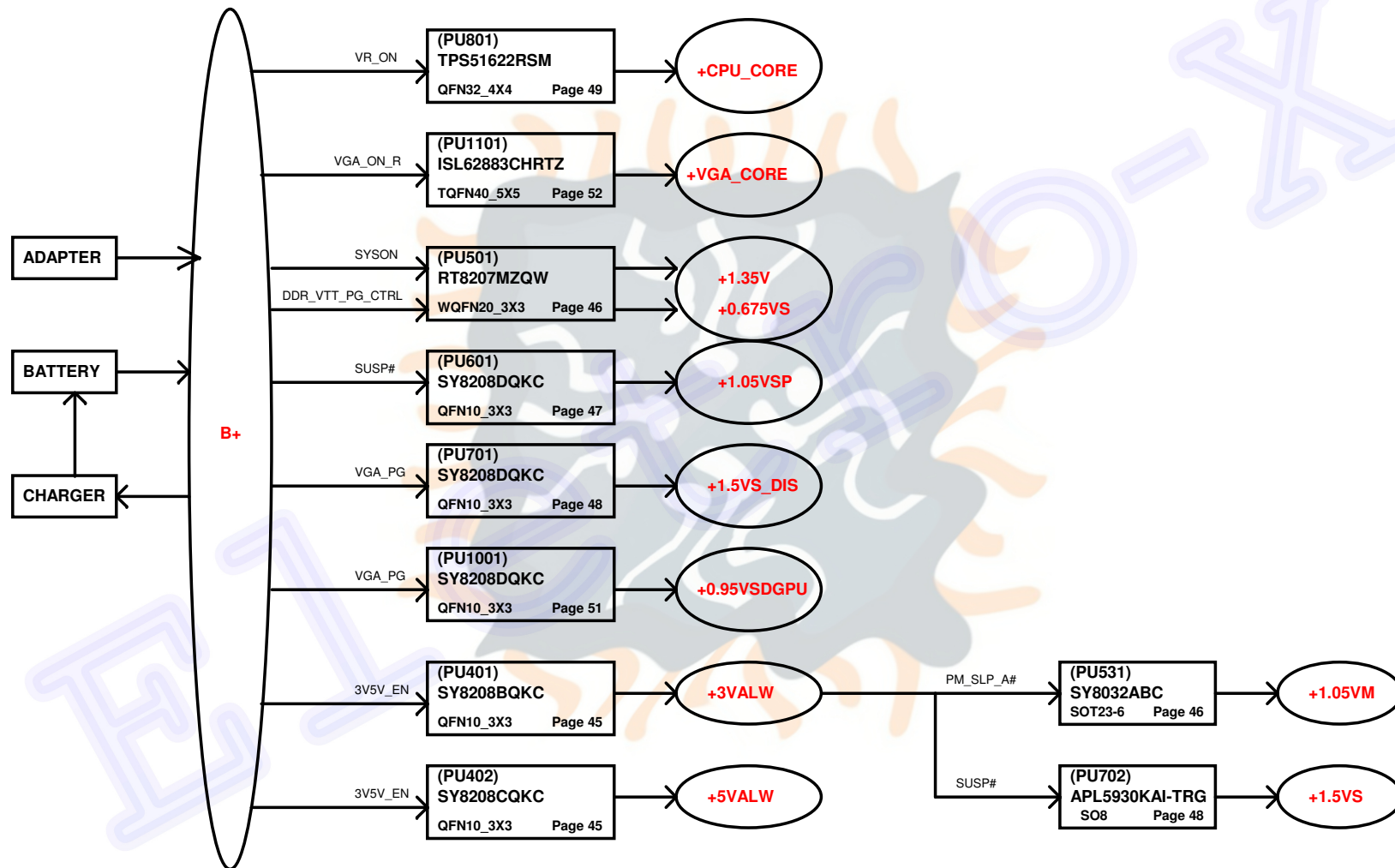
### Broadwell ULT Processor + LP PCH+Nvidia N15S-GT

2014-09-25

Rev : 0 . 4

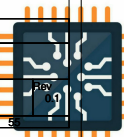
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				LA-B731P
				Date: Thursday, September 25, 2014 Sheet 1

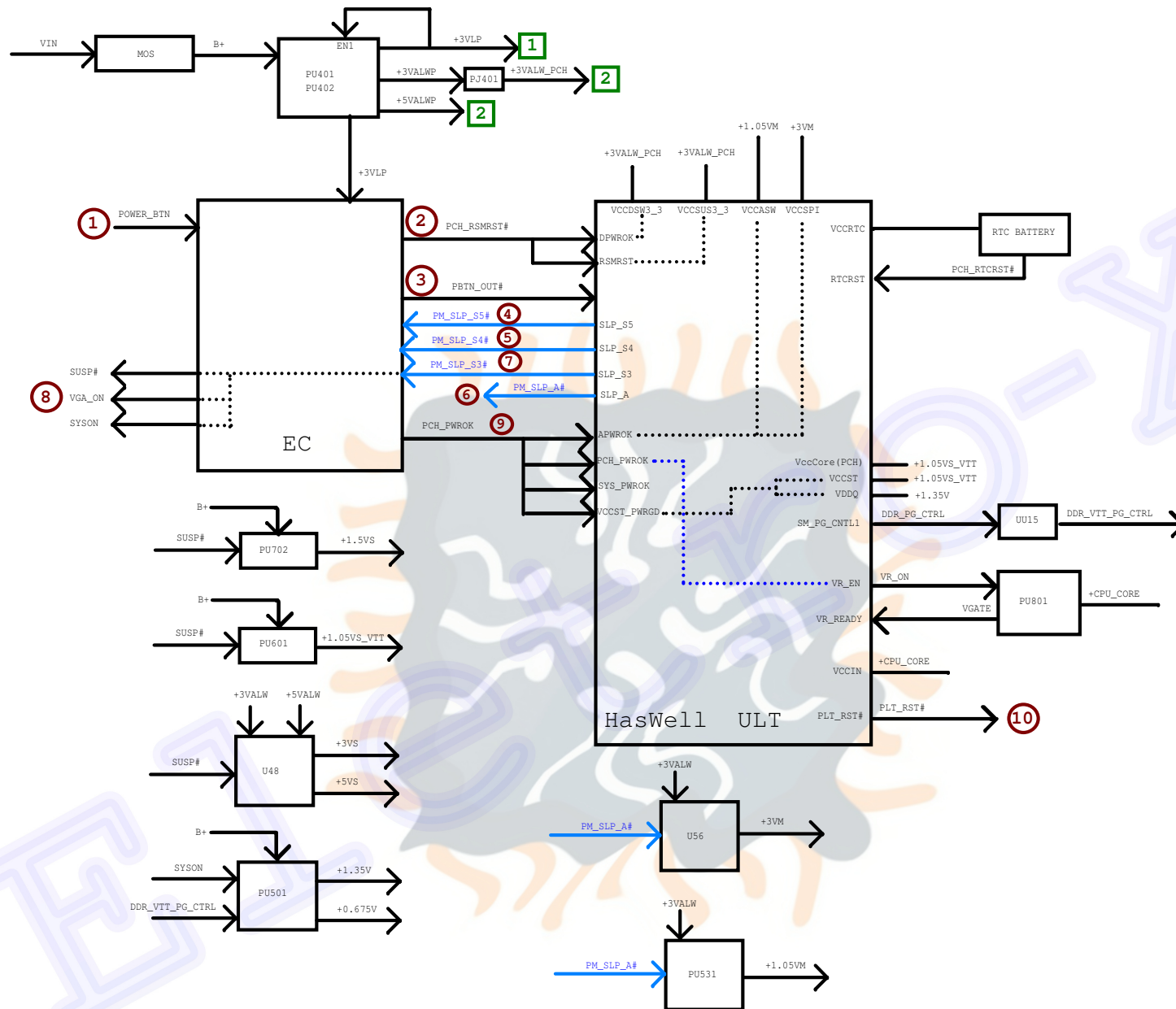




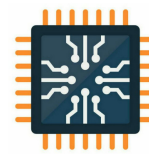
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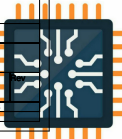
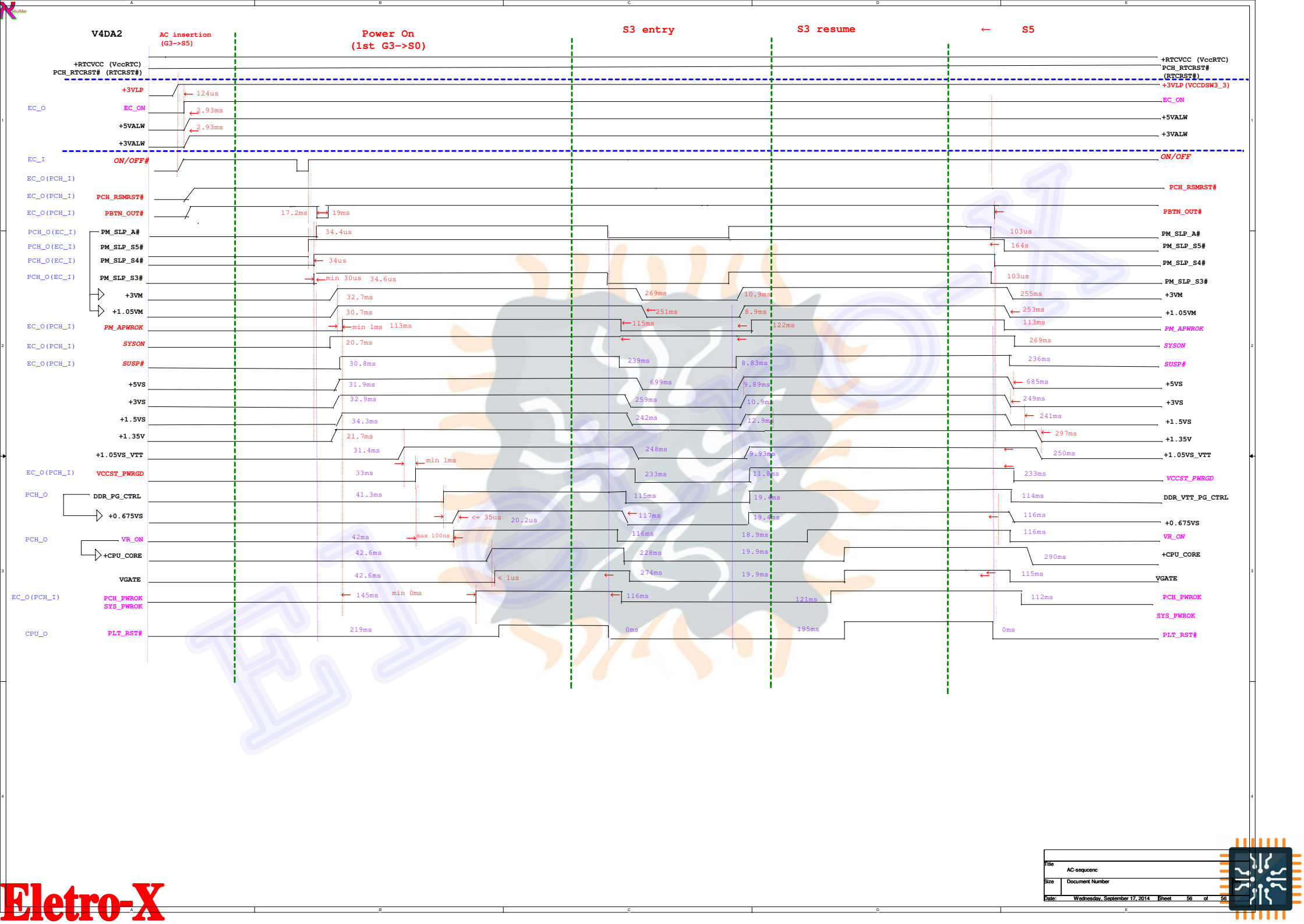
Compal Electronics, Inc.	
Power Tree	
Document Number	Z4DBH M/B LA-B731P Schematic
Date:	Wednesday, September 17, 2014
Sheet	53 of 53



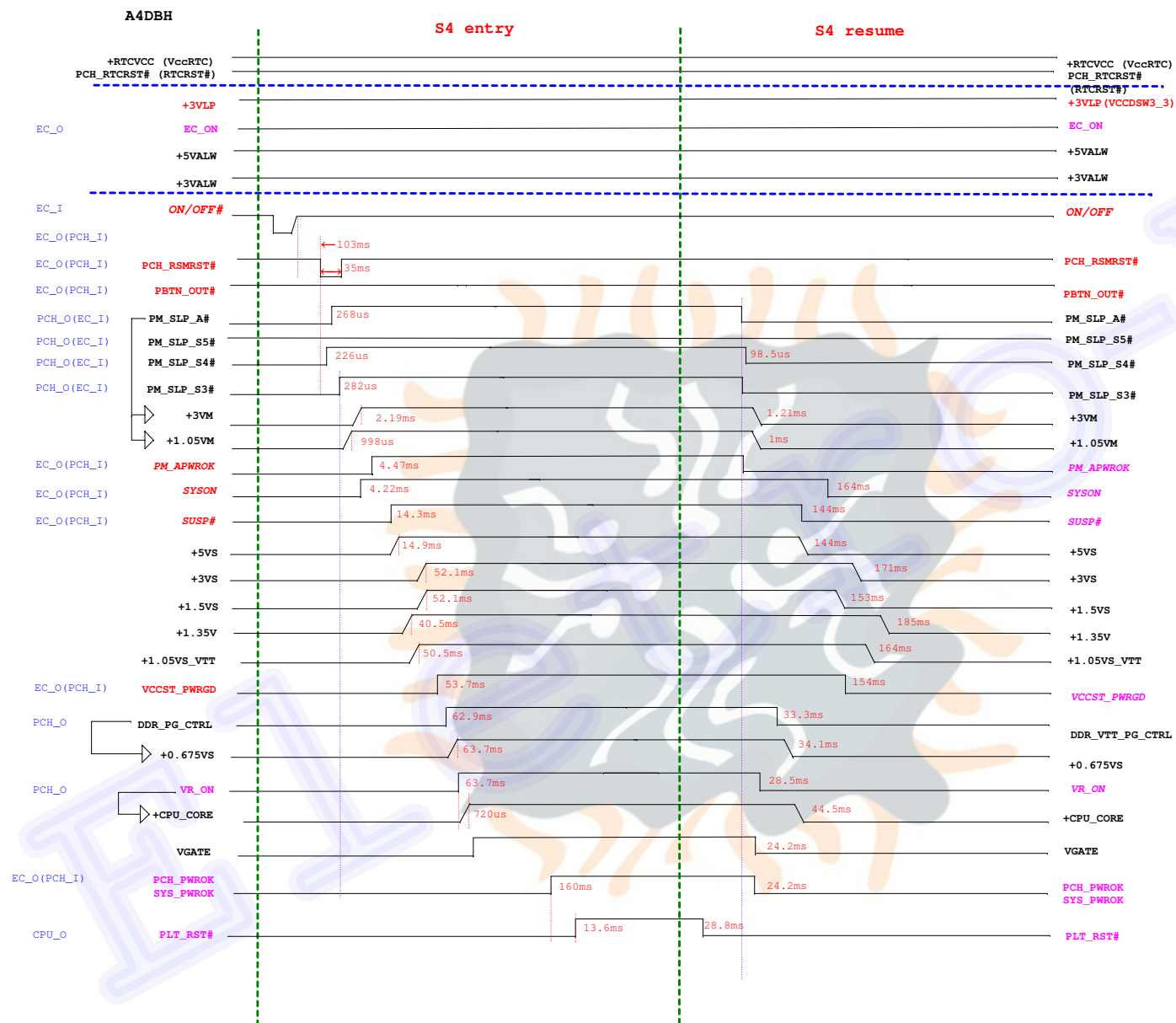


Title		
Power Block		
Size	Document Number	Rev
B	<Doc>	
Date:	Wednesday, September 17, 2014	Sheet 55 of 56









Voltage Rails		S0	AC	AC	AC	DC	DC	DC
Power Plane	Description	S0	AC	AC	AC	DC	DC	DC
+RTCVCC	RTC power	ON	ON	ON	ON	ON	ON	ON
VIN	Adapter power supply (19V)	N/A	ON	ON	ON	OFF	OFF	OFF
BATT+	Battery power supply (9V or 19V)	N/A	N/A	N/A	N/A	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON	ON	ON	ON	ON
+3VALW	+3VALW always on power rail	ON	ON	ON	ON	ON	ON	ON
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH	ON	ON	ON	ON	ON	ON	ON
+3VM	+3VALW to +3VM power rail for PCH	ON	ON*	ON*	ON*	ON*	ON*	ON*
+1.05VM	+1.05VS_VTT to +1.05VM switched power rail for CPU & PCH	ON	ON*	ON*	ON*	ON*	ON*	ON*
+1.05VS_VTT	+1.05VSP to +1.05VS_VTT switched power rail for CPU & PCH	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.35V	+1.35VP to +1.35V switched power rail for DDR terminator	ON	ON	OFF	OFF	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3VS_VGA_AON	+3VS to +3VS_VGA_AON power rail	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+3VS_VGA_MAIN	+3VS to +3VS_VGA_MAIN power rail	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.5VSDGPU	B+ to +1.5VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.05V_VGA	+1.05VS_VTT to +1.5VS_VGA switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+3V_LAN	LAN CHIP POWER RAIL	ON*	ON*	ON*	OFF	OFF	OFF	OFF
+3VS_WLAN	WLAN MODULE POWER RAIL	ON*	ON*	ON*	OFF	OFF	OFF	OFF
+USB3_VCCA	USB Charger PORT0 & PORT9 POWER POWER RAIL	ON	ON	ON	ON	ON*	ON*	ON*
Note : ON* WILL DEPEND ON SLP_A# TO TURN ON OR OFF(ME FIRMWARE CONTROL)								
Note : ON* WILL DEPEND ON BATTERY CAPACITY TO TURN ON OR OFF								
Note : ON** Depend on Optimus ON/OFF.								
Note : ON* Depend on LAN wake SPEC								

#### EC SM Bus1 address

Device	Address
Smart Battery charger IC	0001 011X b
GPU	0001 001X b
	1001 111X b

#### EC SM Bus2 address

Device	Address
On Board Thermal Sensor(CPU)	1001 101xb
PCH	1001_011xb

#### PCH SM Bus address

Device	Address
ChannelA DIMM0	A0 1010 000Xb
ChannelB DIMM0	A4 1010 010Xb
G-sensor	0011 000xb

#### PCH SM Bus0 address

Device	Address
LAN NFC	1100 100xb
	0010_100xb

#### CPU BOM Config

#### RAM BOM Config

HYNIX	256*16	SA00005AV50(H5TC4G63AFR-PBA)	X76SHYNIX0@
ELPDA	256*16	SA00005HT80(EDJ4216EFBG-GNL-F FBGA)	X76SELP0@

#### GPU BOM Config

N15S-GT	SA00007GJ00 (S IC N15S-GT-S-A2 BGA 595P GPU)
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#### VRAM BOM Config

HYNIX	256*16	SA00006E800(H5TC4G63AFR-11C FBGA 96P)	X76VHYNIX0@
SAMSUNG	256*16	SA000076P00(K4W4G1646D-BC1A FBGA 96P)	X76VSAM0@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

#### Board ID / SKU ID Table for AD channel

+3VALW_EC	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B

#### USB Port Table

USB 2.0	Port	USB Port
EHCI	0	USB Port 3.0 (I/O board)
	1	USB port 3.0 (Left side)
	2	DOCK USB3.0
	3	USB Port 3.0 (I/O board)
	4	Camera
	5	Mini Card(3G)
	6	Mini Card(WLAN+BT)
	7	Finger Print

USB 3.0	Port	
XHCI	1	USB Port 3.0 (I/O board)
	2	USB3 (Left side)

#### PCIe Table

Port	PCI Express Port
1	USB 3.0 DOCK
2	USB 3.0 (I/O board)
3	LAN
4	WLAN
5-L0	VGA
5-L1	
5-L2	
5-L3	CardReader
6-L0	

#### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

#### BTO Option Table

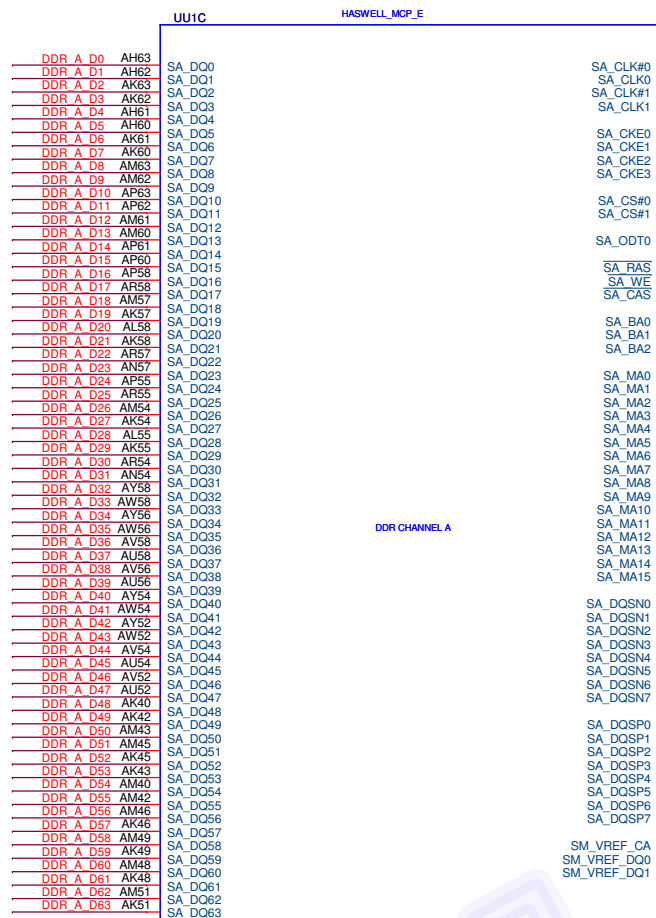
BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA Only	UMA@
DISCRETE	VGA@
DRAM ELPIDA	X76SELP0@
DRAM HYNIX	X76SHYNIX0@
NFC Function	NFC@
3G Function	3G@
VPRO Function	VPRO@
NO VPRO Function	NOVPRO@
EMI SOLUTION	EMI@
UMA Part Count	PC@
SATA RE-DRIVER	SD@
ESD SOLUTION	ESD@
VRAM HYNIX	X76VHYNIX0@
VRAM SAMSUNG	X76VSAM0@
EC 9012	9012@
EC 9022	9022@
GC6 Function	GC6@
No GC6 Function	NOGC6@
TI re-driver	X76TI@
Parade re-driver	X76PAR@

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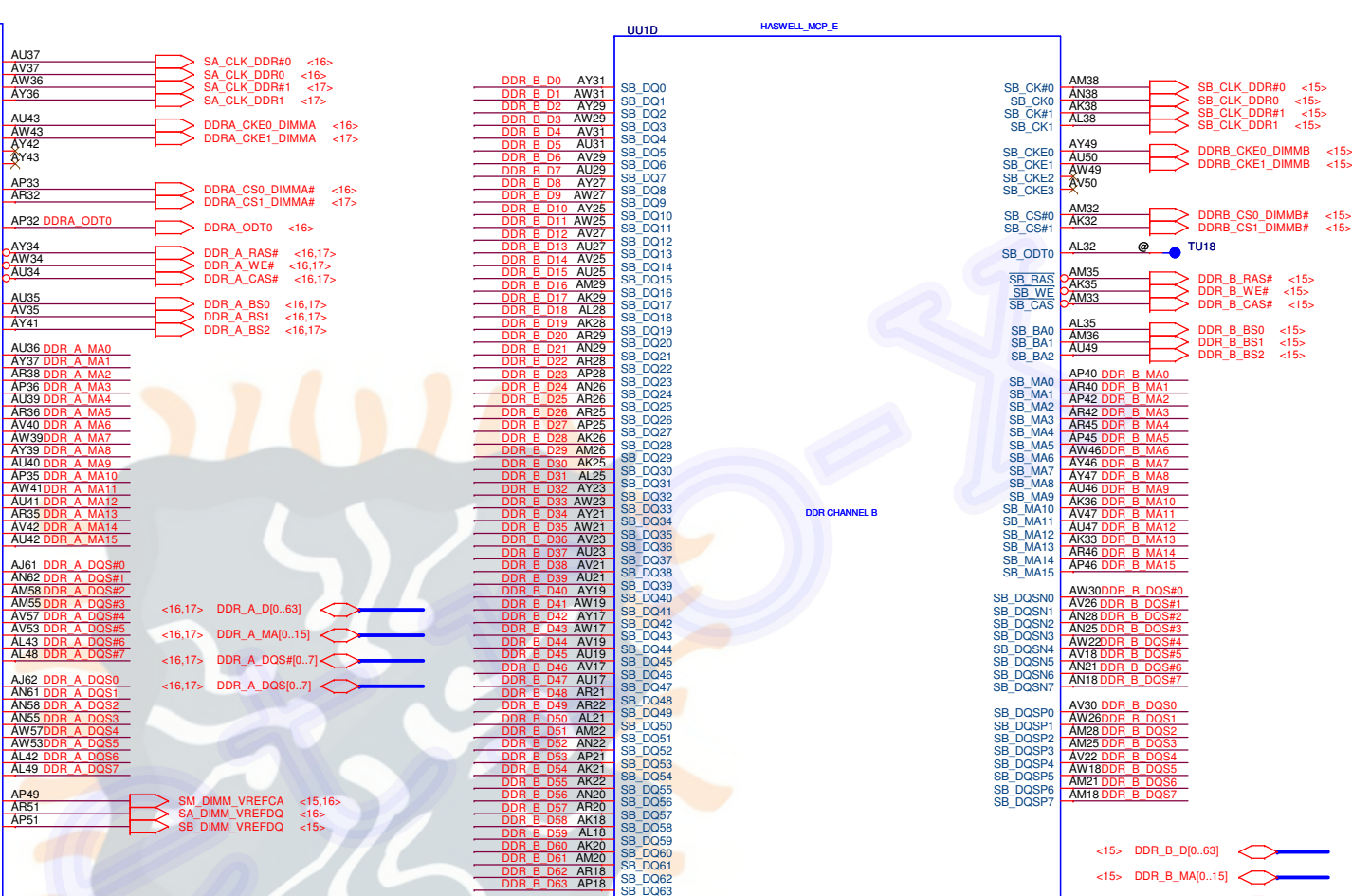




HASWELL-MCP-E-ULT BGA1168

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Rev1p2

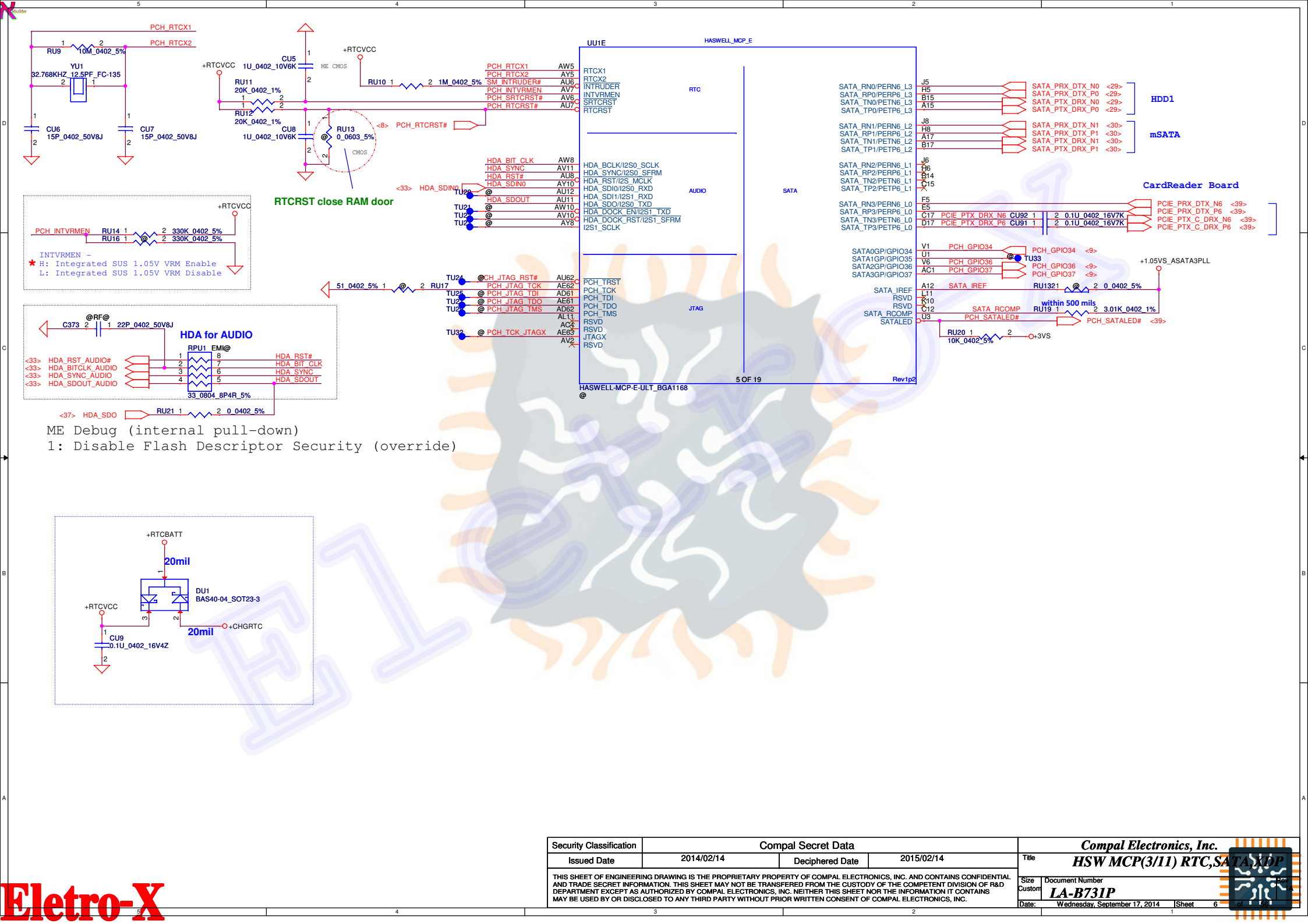


1. *Journal of Management Studies*, 1997, 34, 1, 1-14.

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Rev1p2

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>HSW MCP(2/11) DDRIII</b>	
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ME Debug (internal pull-down)  
1: Disable Flash Descriptor Security (override)

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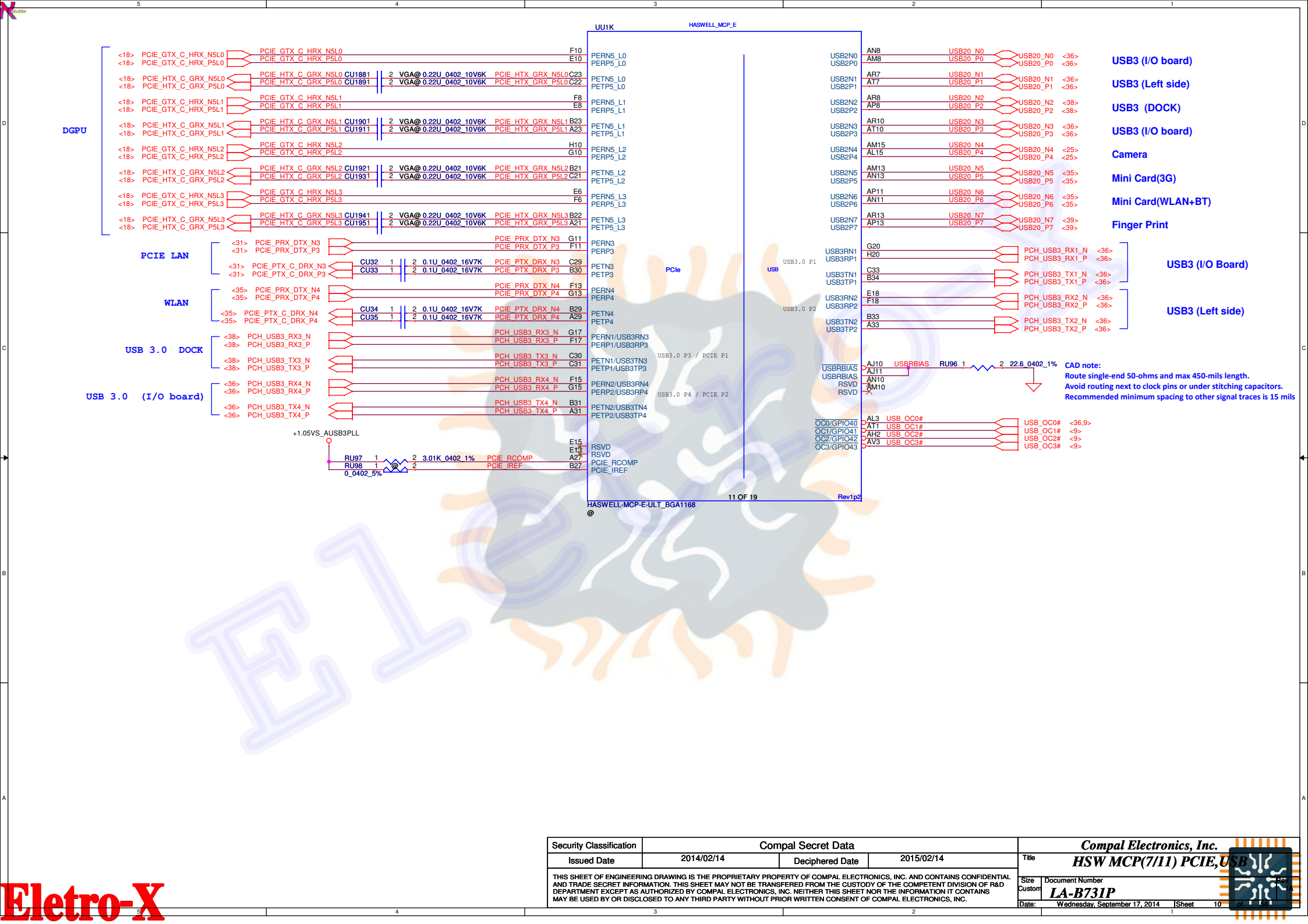












DGPU

PCIE LAN

WLAN

USB 3.0 DOCK

USB 3.0 (I/O board)

USB3 (I/O board)

USB3 (Left side)

USB3 (DOCK)

USB3 (I/O board)

Camera

Mini Card(3G)

Mini Card(WLAN+BT)

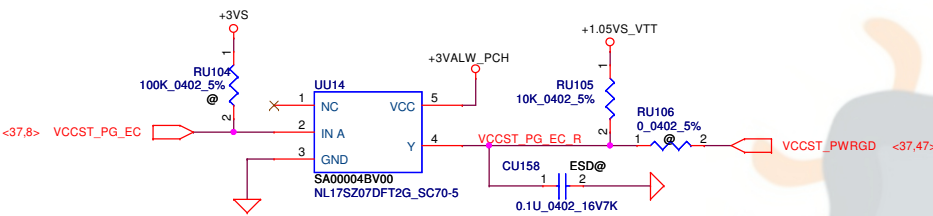
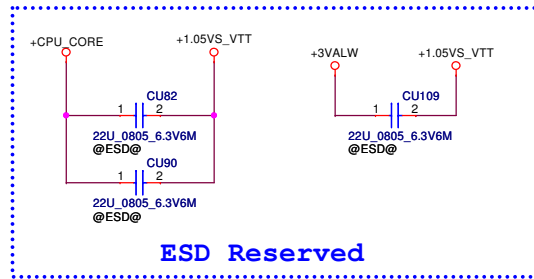
Finger Print

USB3 (I/O Board)

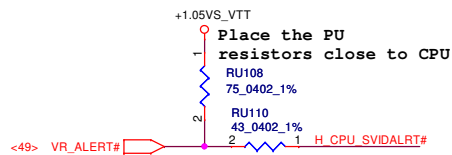
USB3 (Left side)

CAD note:  
Route single-end 50-ohms and max 450-mils length.  
Avoid routing next to clock pins or under stitching capacitors.  
Recommended minimum spacing to other signal traces is 15 mils

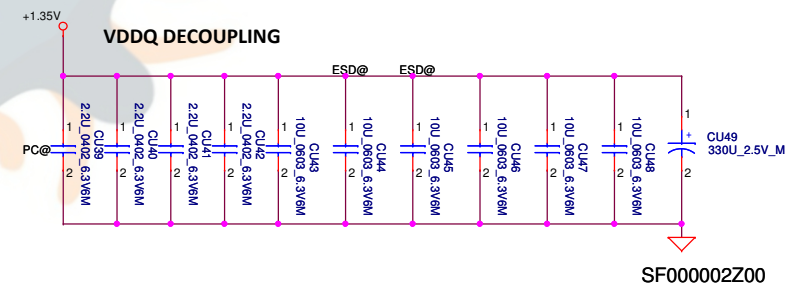
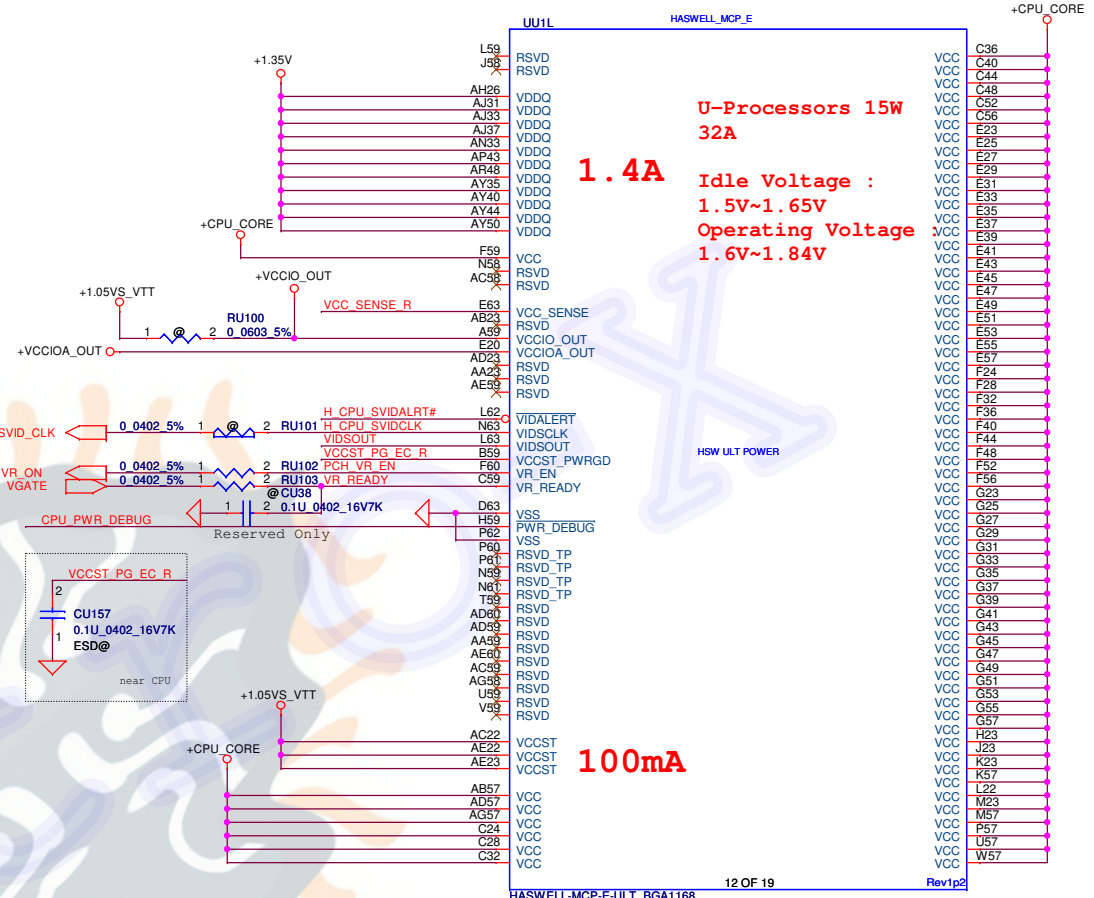
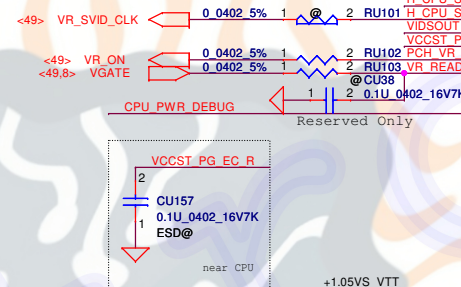
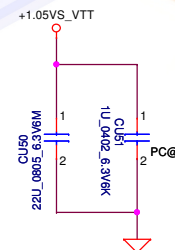
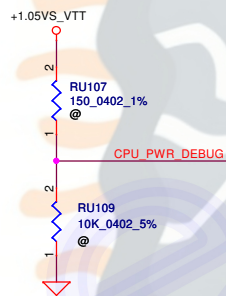
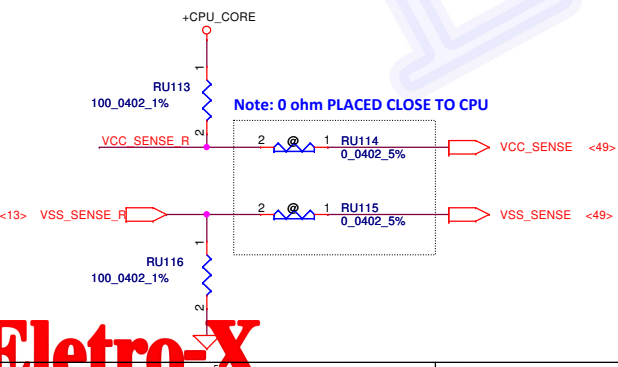
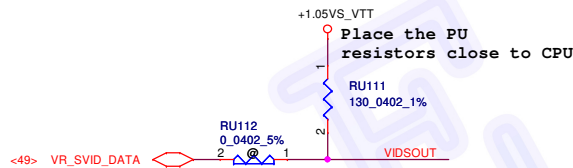
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				HSW MCP(7/11) PCIE,USB	
				Size	
				Document Number	
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				Sheet 10	



## SVID ALERT



## SVID DATA



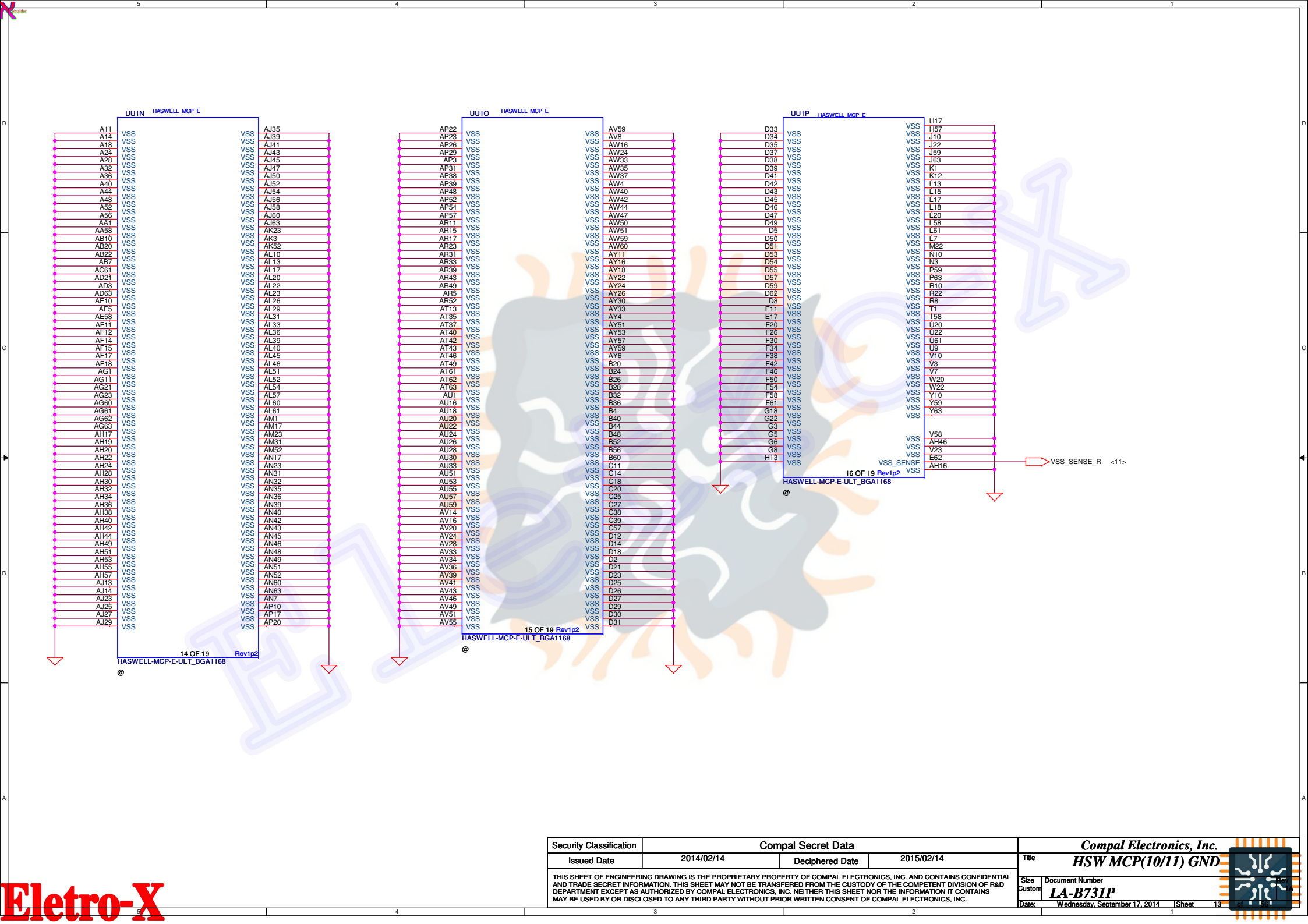
+1.35V : 470UF/2V/7343 \* 2  
 10UF/6.3V/0603 \* 6  
 2.2UF/6.3V/0402 \* 4

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				Size	
				Document Number	
				LA-B731P	
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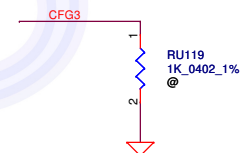
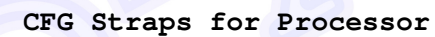
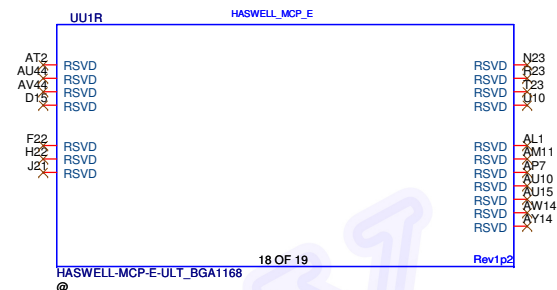




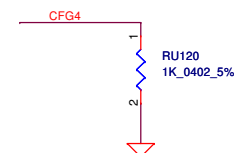




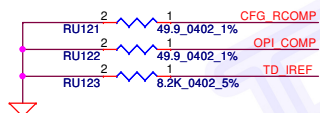
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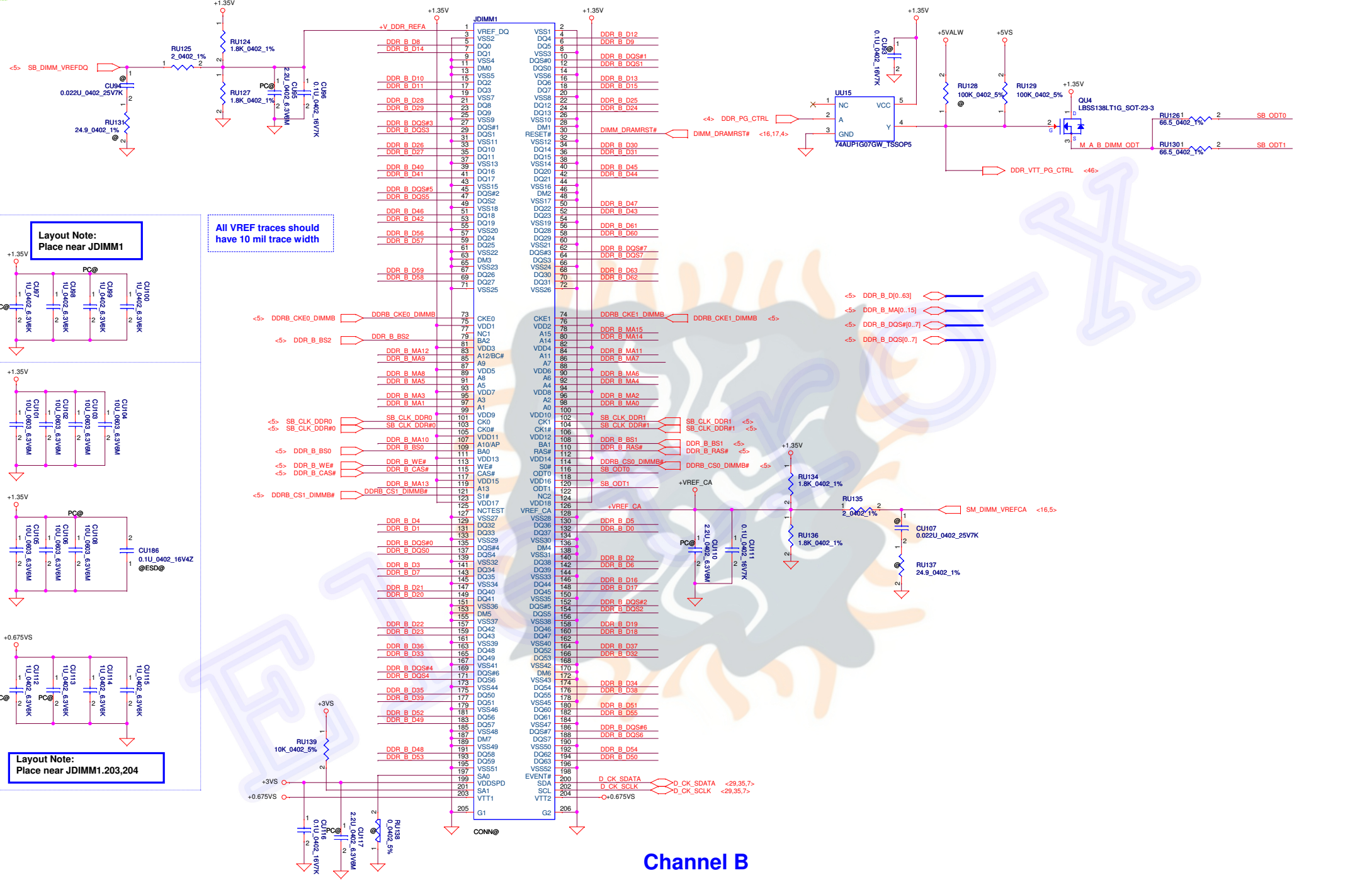


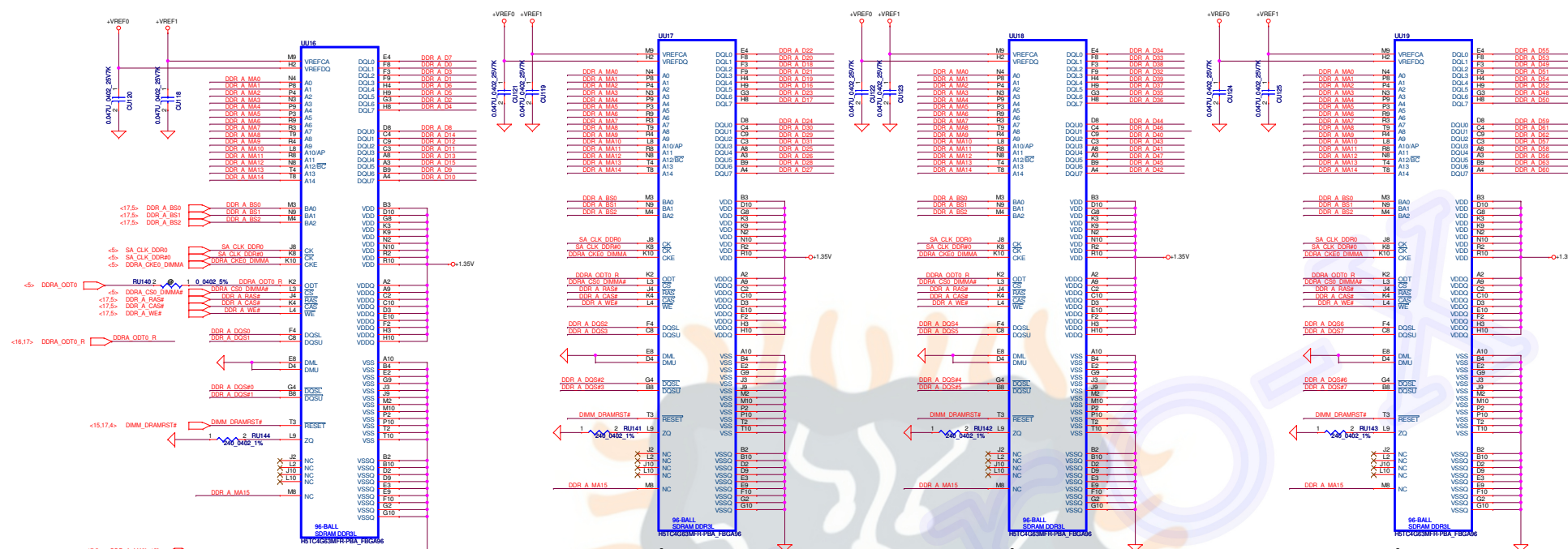
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



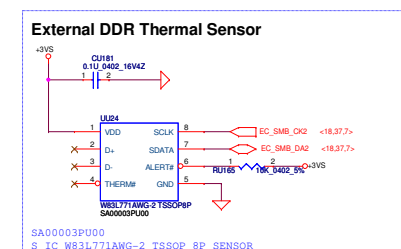
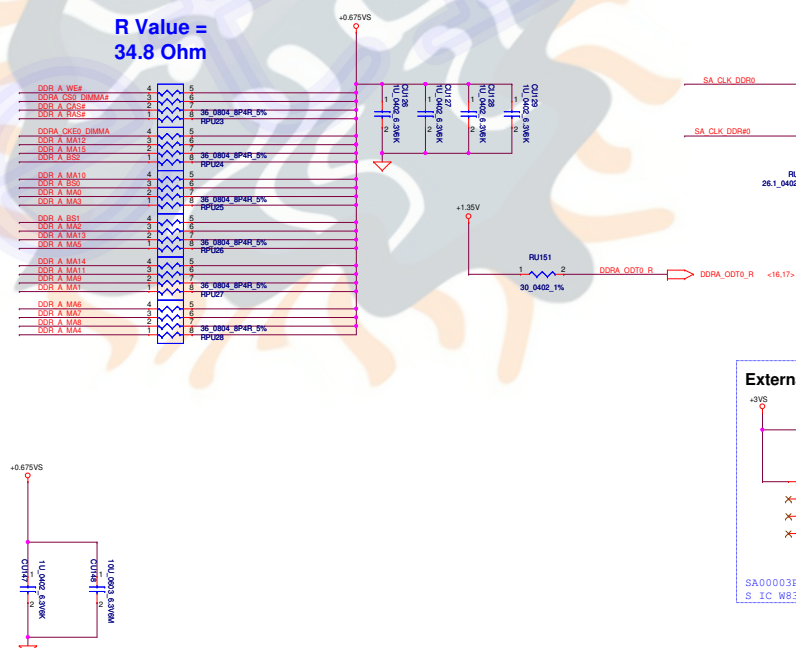
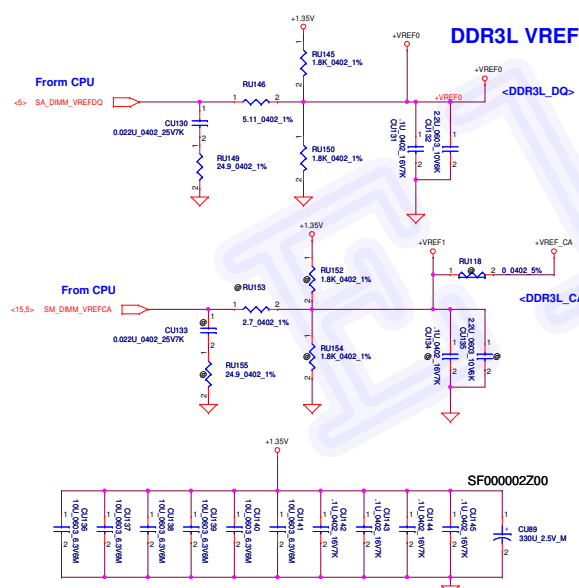
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



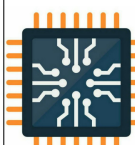




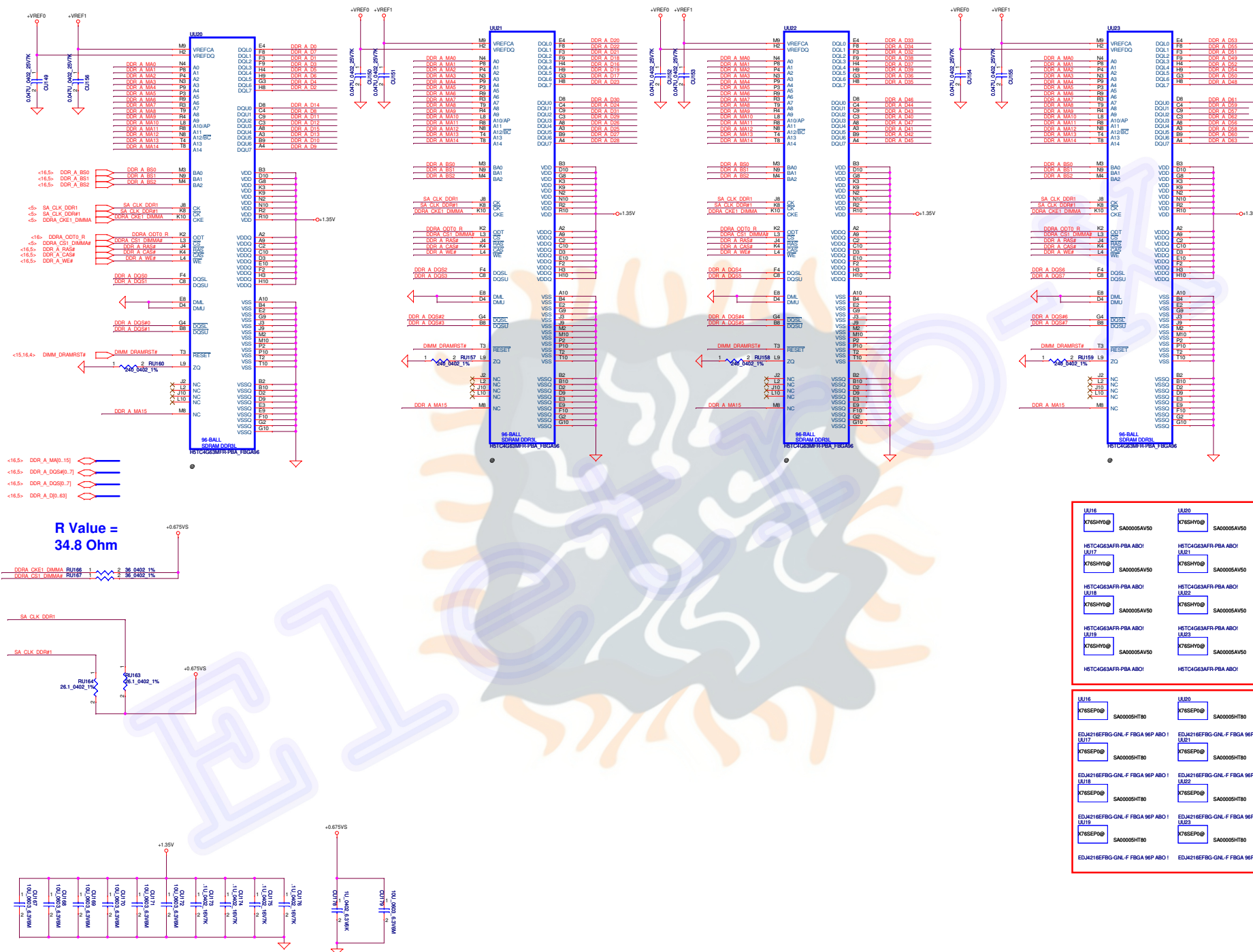
**R Value =  
34.8 Ohm**



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DocID Number	DDRIH ON BOARD CHIPS	DocID Number	DDRIH ON BOARD CHIPS







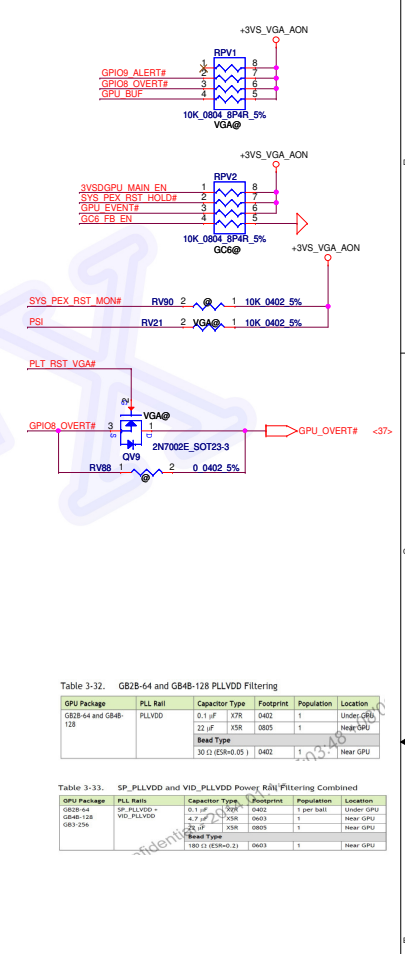
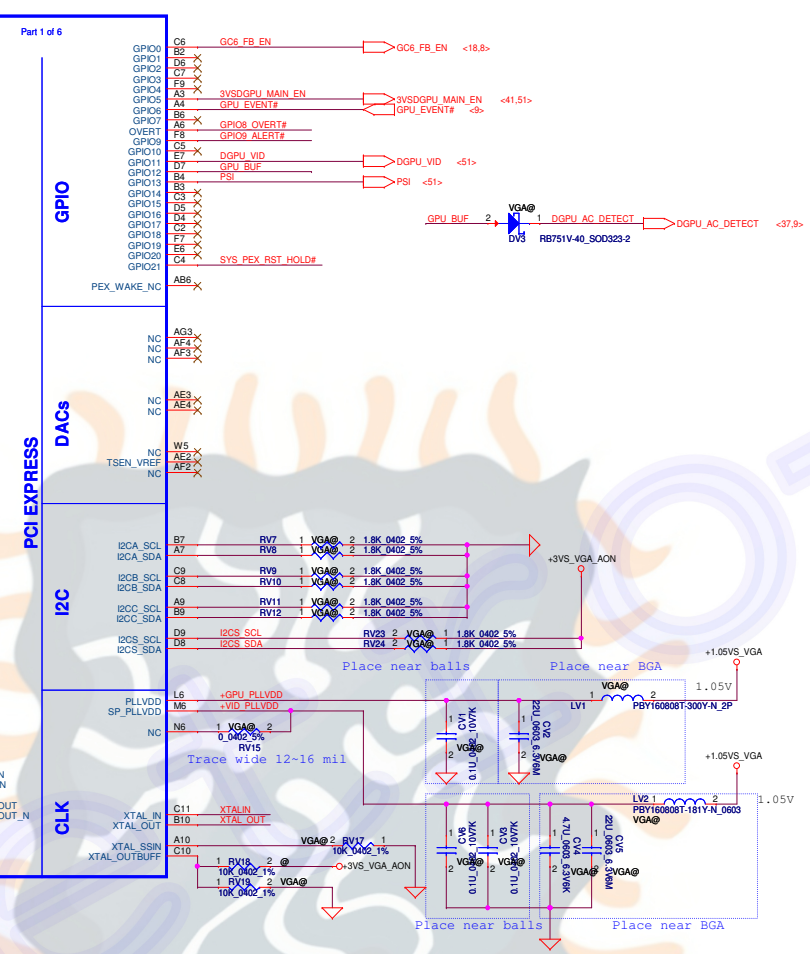
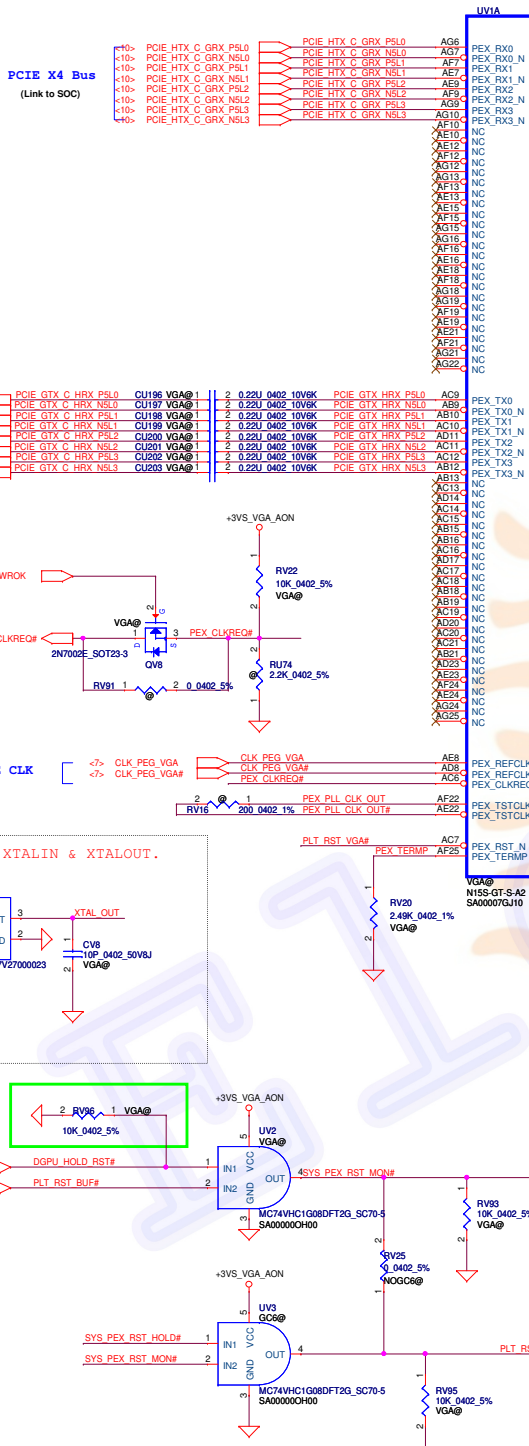
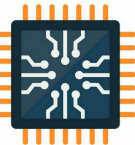


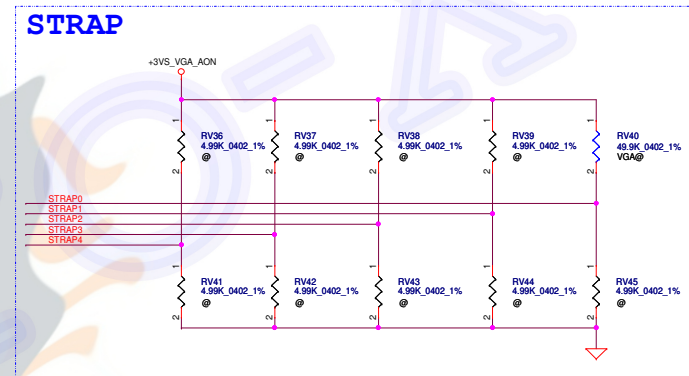
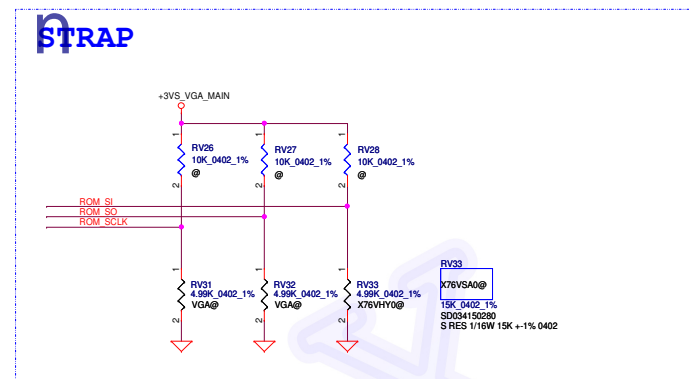
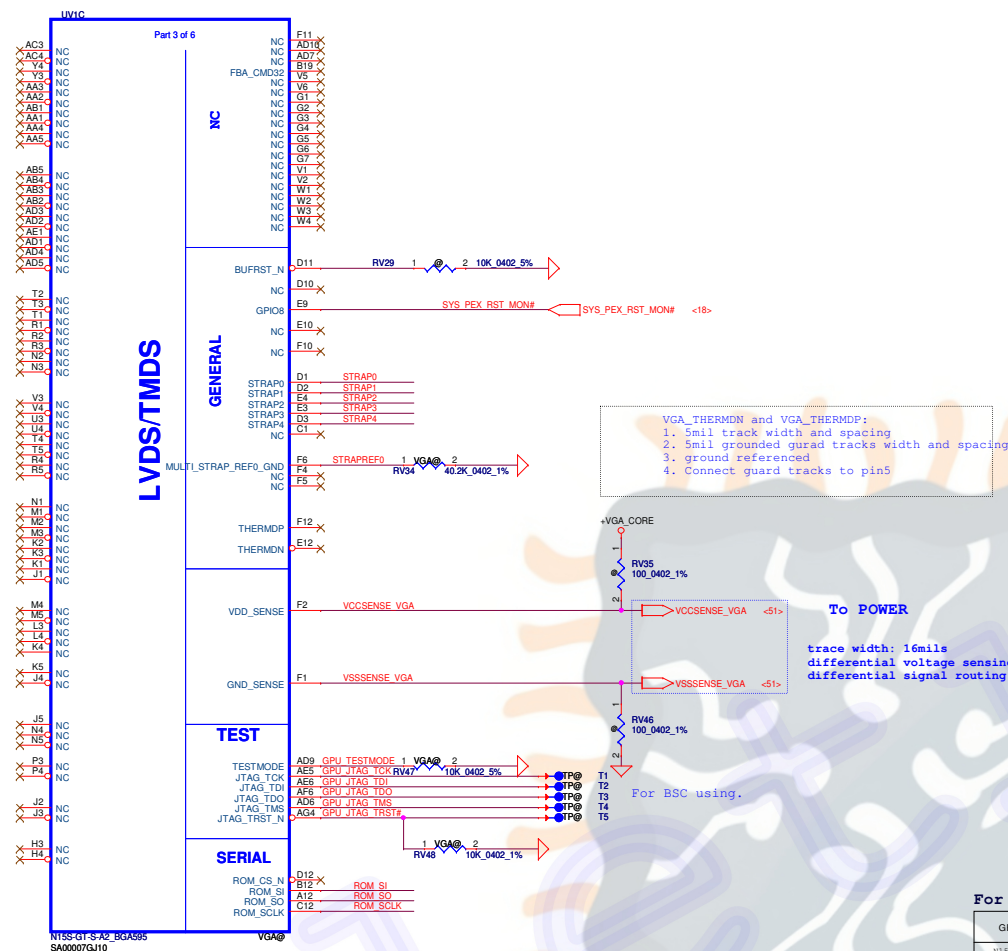
Table 3-32. GB28-64 and GB48-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB28-64 and GB48-128	PLLVDD	0.1 μF	XSR	0402	Under GPU
		22 μF	XSR	0805	1
		Bead Type	30 Ω (ESR<0.05 Ω)	0402	1
					Near GPU

Table 3-33. SP\_PLLVDD and VID\_PLLVDD Power RAIL Filtering Combined

GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB28-64 and GB48-128	SP_PLLVDD	0.1 μF	XSR	0402	Under GPU
		4.7 μF	XSR	0805	1
		Bead Type	25 Ω (ESR<0.05 Ω)	0402	1
					Near GPU





For N155-GTstrap table

GPU	Freqz	Memory Size	Memory Config	Strap	BitX	ROM_SI
N155-GT	1000 MHz	256M 16*4 2G	Hynix H5TC4G63AFR-11C	0x0	0 0 0 0	R PD 4.99K
N155-GT	1000 MHz	256M 16*4 2GB	Samsung K4W4G1646D-BC1A	0x2	0 0 1 0	R PD 15K

GB2B-64 Multi-Level Mode

Strap Pin Name	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_MAIN	SOR3_EXPOSED(*0)	SOR2_EXPOSED(*0)	SOR1_EXPOSED(*0)	SOR0_EXPOSED(*0)
ROM_SI	+3VS_MAIN	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_MAIN	DEVID_SEL(*0)	PCIE_CFG(*0)	SMB_ALT_ADDR(0*)	VGA_DEVICE(*0)
STRAP0	Keep foot print for pull up to 3V3_AON an pull down to GND and stuff 50 k ohm pull up				
STRAP1	Keep foot print for pull up to 3V3_AON an pull down to GND for forward compatibility				
STRAP2					
STRAP3					
STRAP4					

Resistor Values (1%)	Pull-up to +3VS_MAIN	Pull-down to Gnd
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

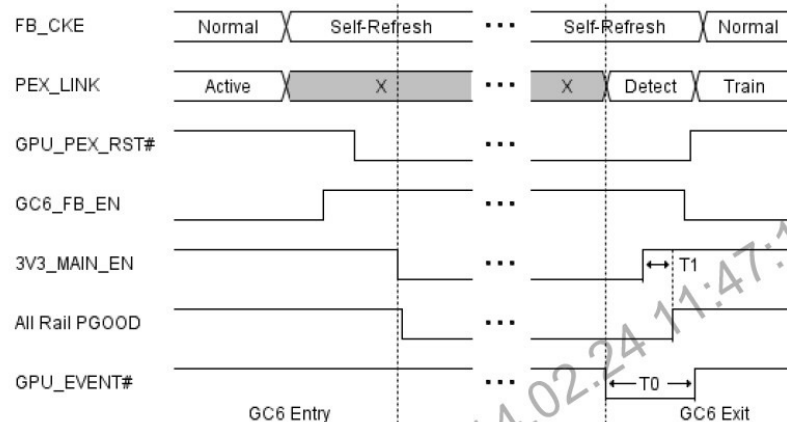


Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram



GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 (D03)	0.1 $\mu$ F	X7R 0402	2	Under GPU
	1 $\mu$ F	X7R 0603	2	Under GPU
	4.7 $\mu$ F	X6S 0603	2	Under GPU
	10 $\mu$ F	X5R 0805	1	Near GPU
	22 $\mu$ F	X5R 0805	1	Near GPU

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0 $\mu$ F	X6S 0402	1	Under GPU
	4.7 $\mu$ F	X6S 0603	1	Near GPU
	10 $\mu$ F	X5R 0805	1	Midway between GPU and Power Supply
	22 $\mu$ F	X5R 0805	1	Midway between GPU and Power Supply

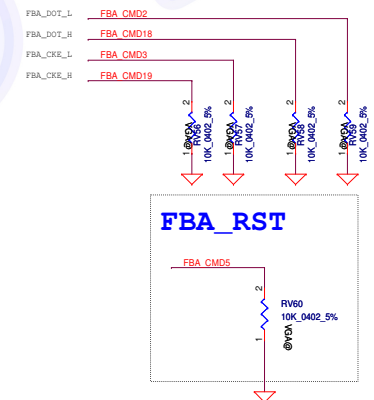
GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_MAIN	0.1µF	X6S 0402	2	Under GPU
GB4B-128		1µF	X5R 0603	1	Near GPU
GB3-256		4.7µF	X5R 0603	1	Near GPU
GB2B-64	3V3_AON	0.1µF	X6S 0402	1	Under GPU
GB4B-128		1µF	X5R 0603	1	Near GPU
GB3-256		4.7µF	X5R 0603	1	Near GPU

Capacitor Type	Footprint	Population	Location	
0.1 $\mu$ F	X5R	0402	1	Near GPU
4.7 $\mu$ F	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 $\mu$ F	X6S	0402	1	Under GPU
1.0 $\mu$ F	X5R	0603	1	Near GPU
4.7 $\mu$ F	X5R	0805	1	Near GPU







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<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
C	<b>LA-B731P</b>		0.1

# Memory Partition A - Lower 32 bits [31..0]

Table 6-3 lists the Mode D command mapping and Table 6-4 on page 91 lists Mode E.

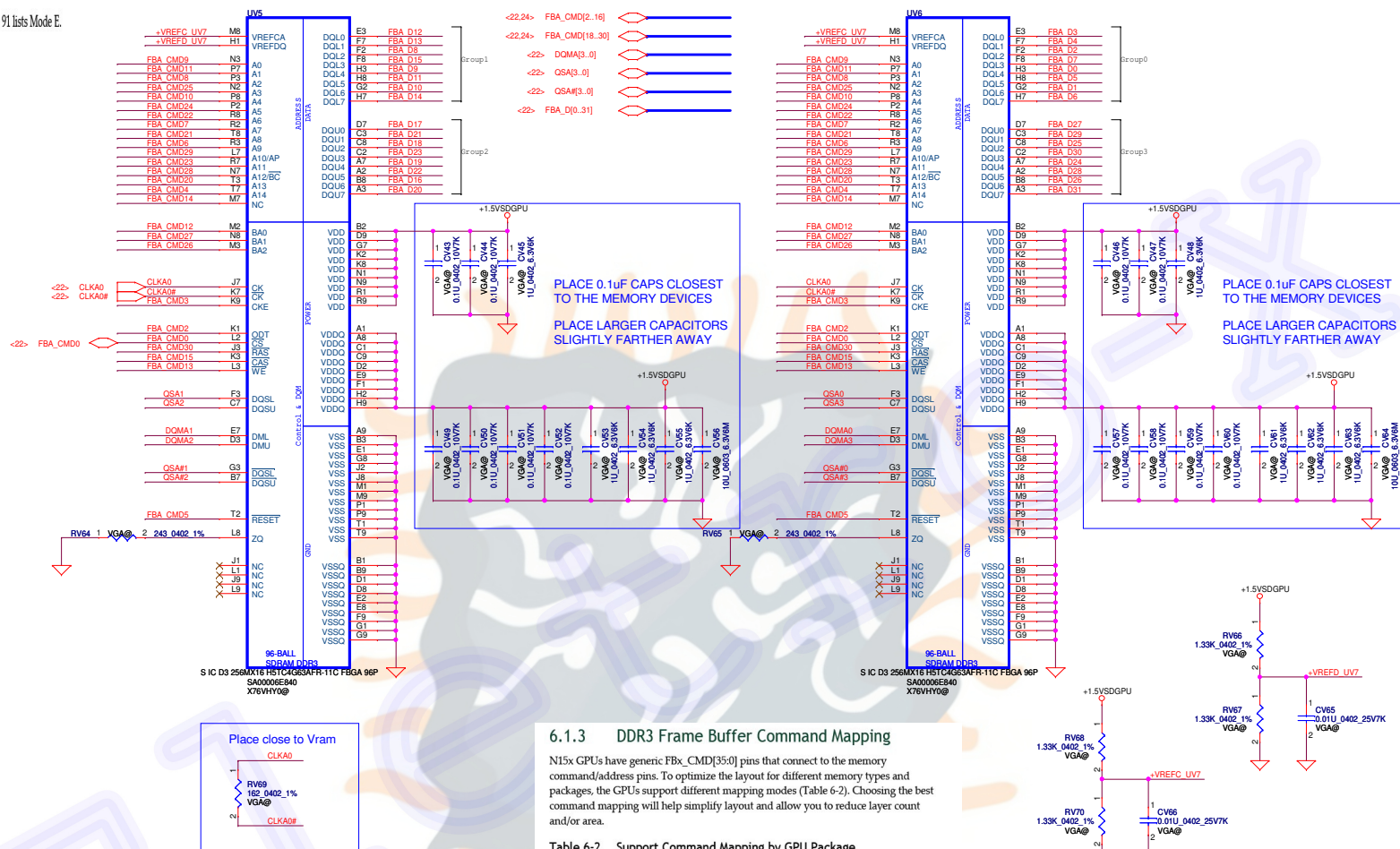
Table 6-3. Mode D Command Mapping

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FbX_CMD0	CS0*	
FbX_CMD1		
FbX_CMD2	ODT	
FbX_CMD3	CKE	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE*	WE*
FbX_CMD14	A15	A15
FbX_CMD15	CAS*	CAS*

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FbX_CMD16	CS0*	
FbX_CMD17		
FbX_CMD18	ODT	
FbX_CMD19	CKE	
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RAS*	RAS*
FbX_CMD31		
FbX_CMD32		
FbX_CMD33 <sup>1</sup>		
FbX_CMD34	DBG0 <sup>2</sup>	
FbX_CMD35	DBG1 <sup>2</sup>	

Notes:

1. Not available in GB2B-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11



## 6.1.3 DDR3 Frame Buffer Command Mapping

N15x GPUs have generic FBx\_CMD[35:0] pins that connect to the memory command/address pins. To optimize the layout for different memory types and packages, the GPUs support different mapping modes (Table 6-2). Choosing the best command mapping will help simplify layout and allow you to reduce layer count and/or area.


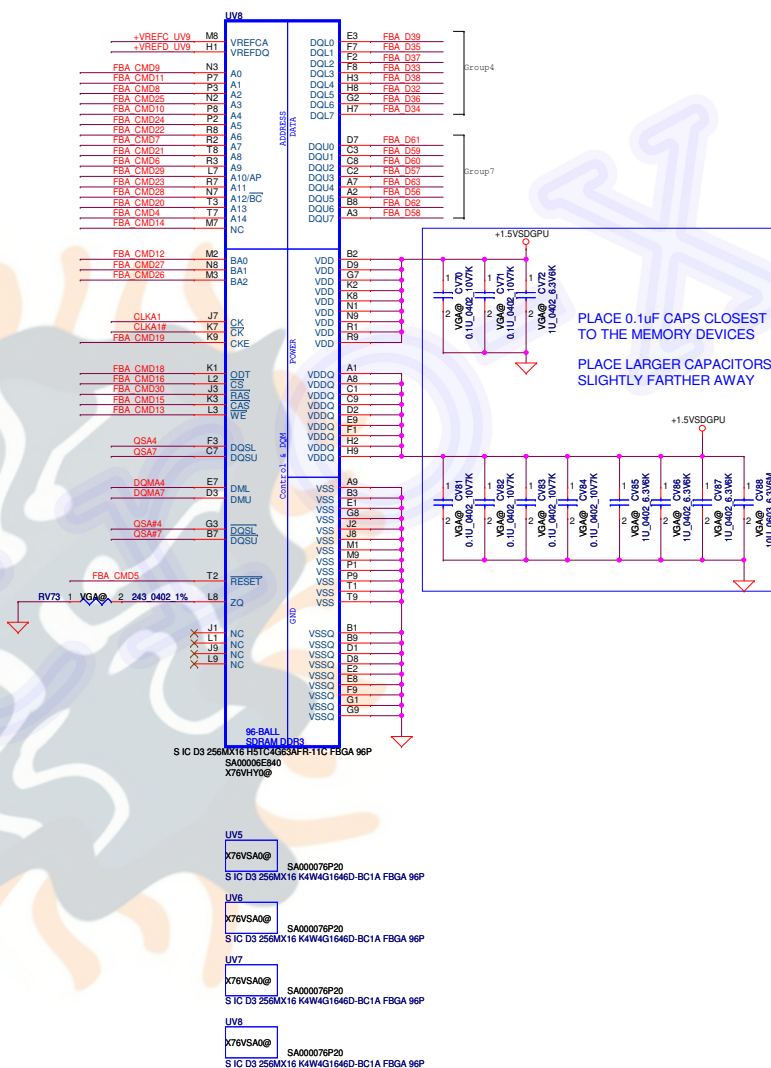
Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2B-64 GB4B-128	D	Mode D is optimized for H15x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers. This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2B-64 GB4B-128	E	Mode E is optimized for DDR3 dual rank designs.

Note: \*Not including two additional layers for power planes.

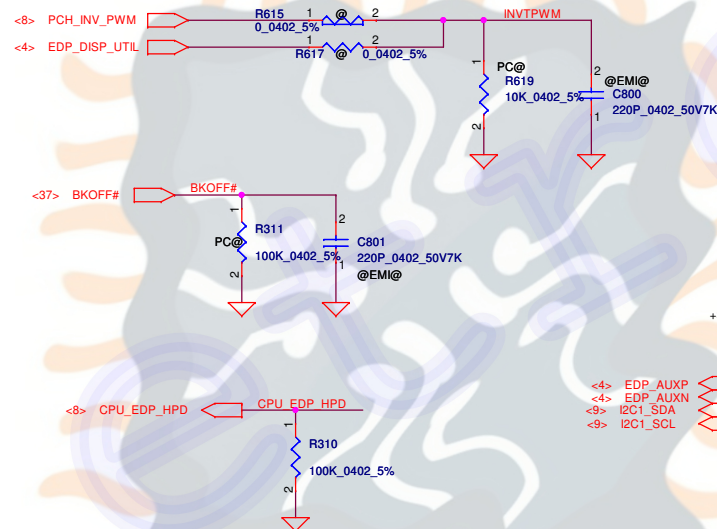
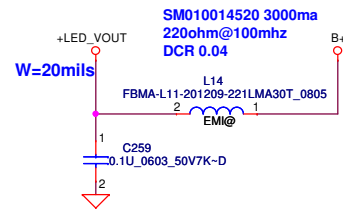
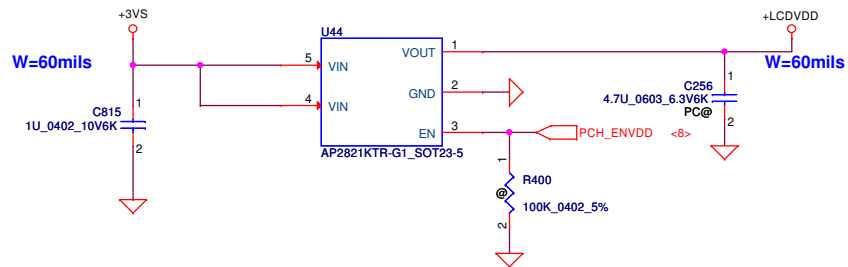


# Eletro-X

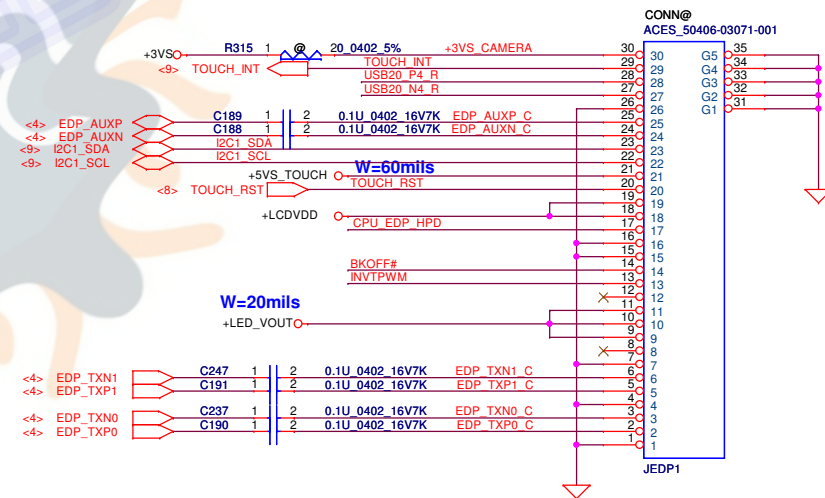




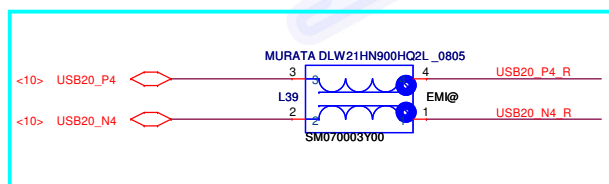
## LCD POWER CIRCUIT



## eDP PANEL Conn.



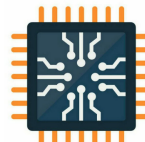
## Camera



(EMI request)

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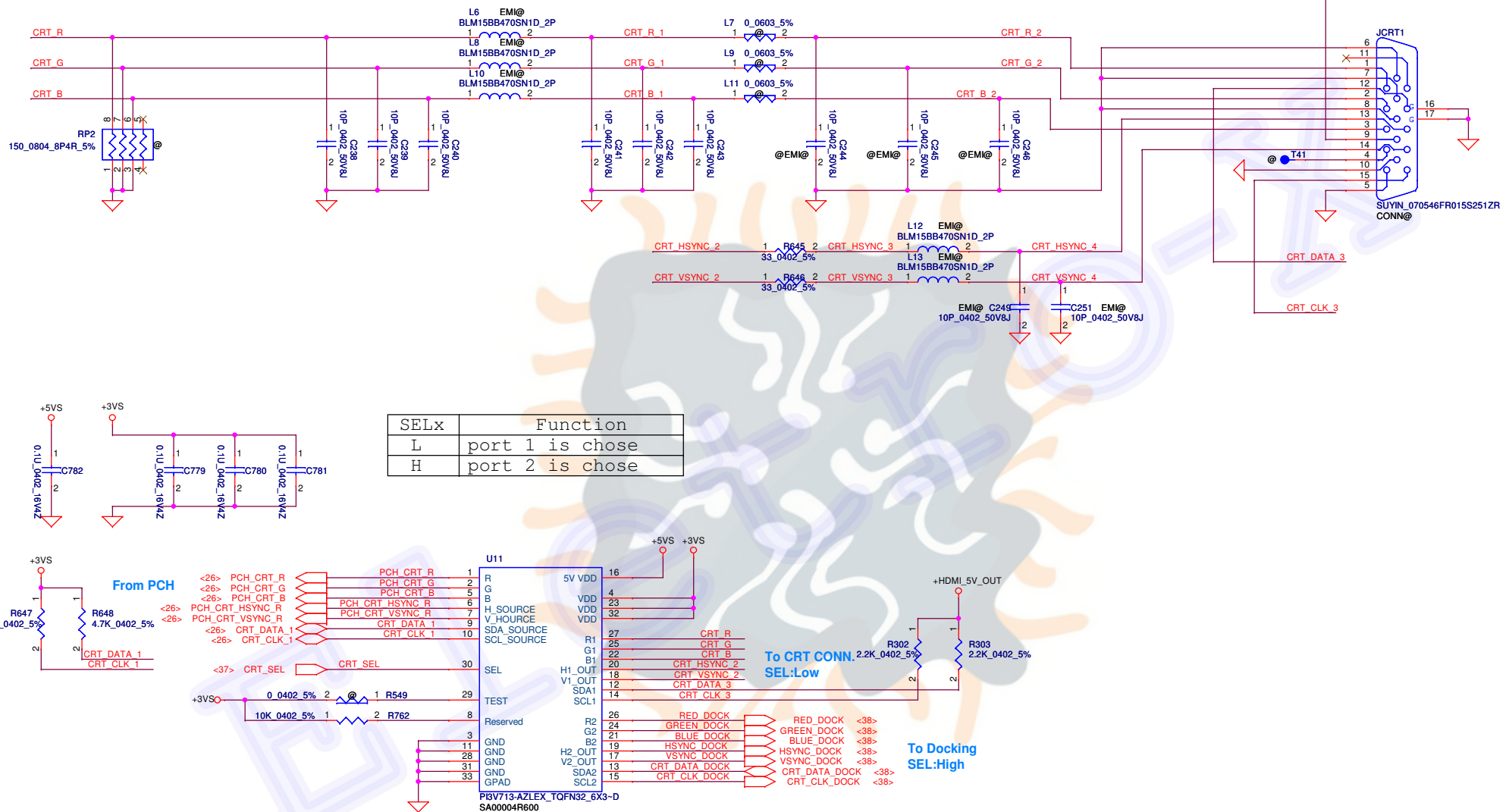
# Eletro-X



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# CRT Connector

CRB1.0 use 47ohm@100Mhz Bead

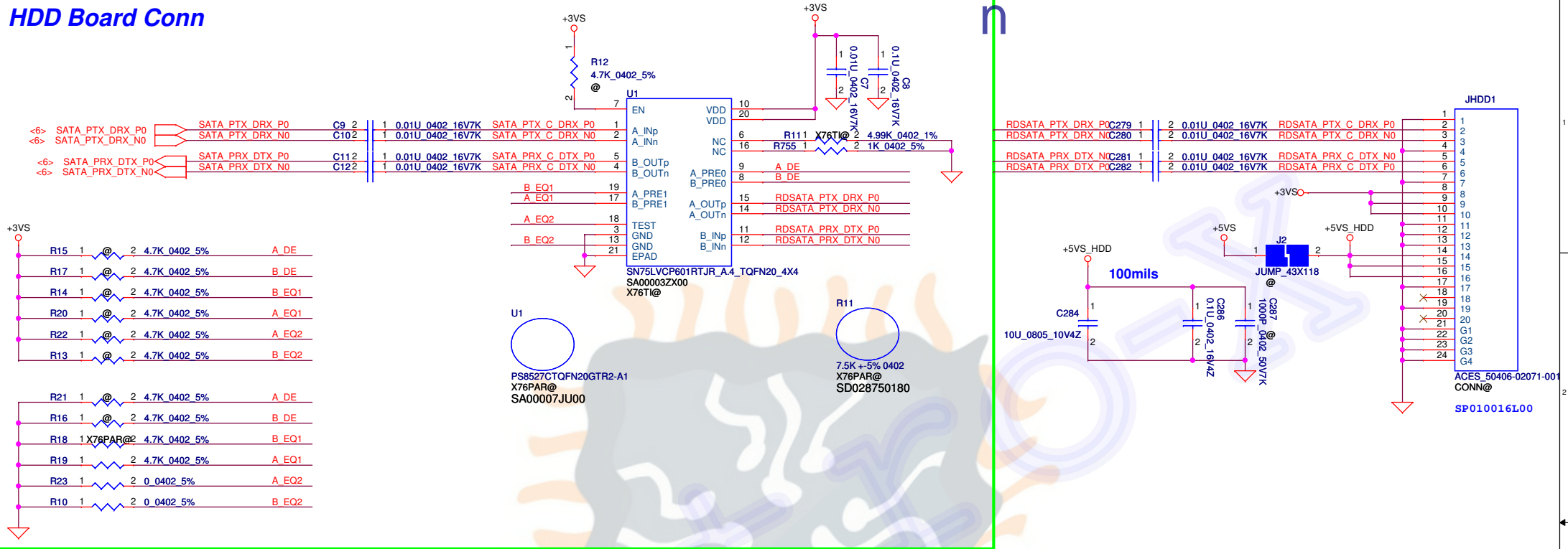


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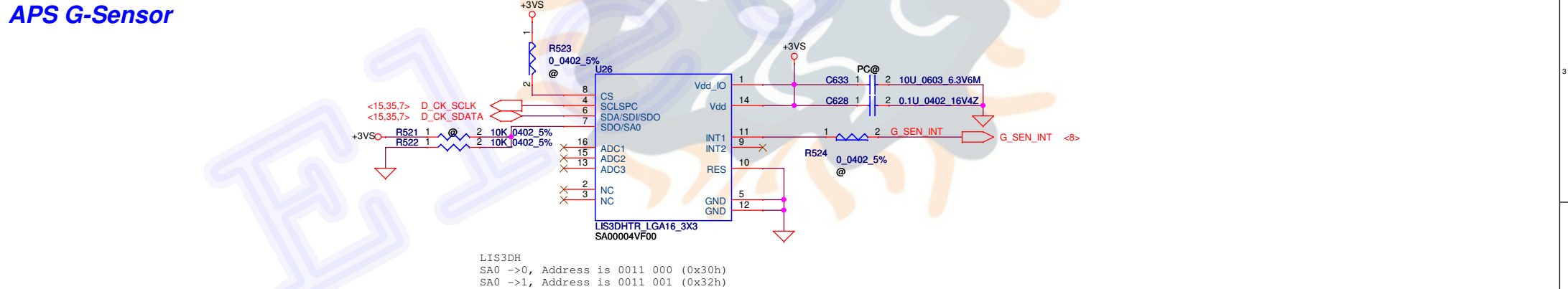




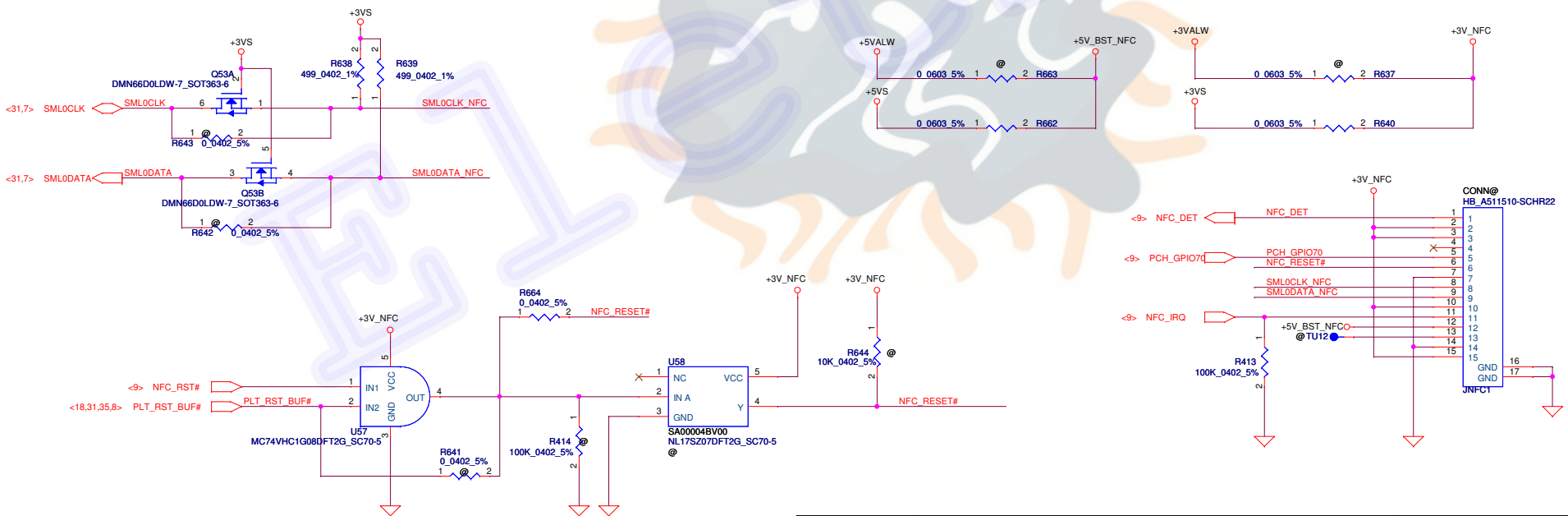
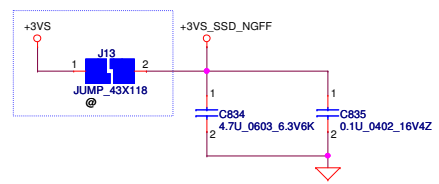
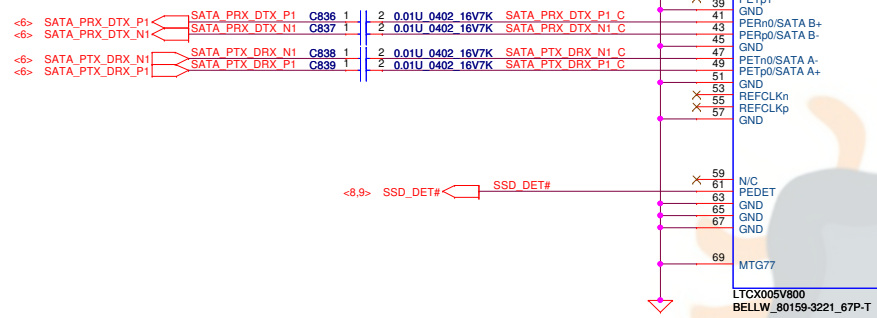
## HDD Board Conn



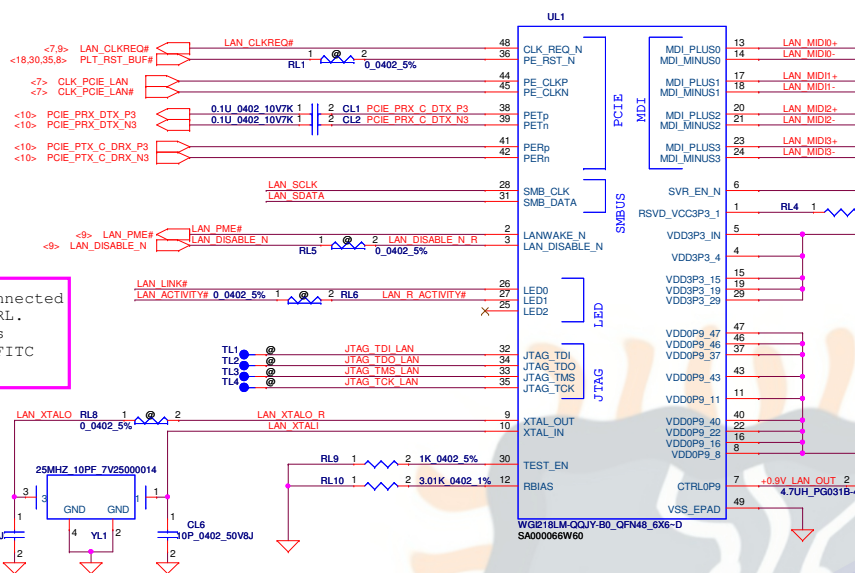
## APS G-Sensor



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NOTE: LANWAKE\_N must be connected to PCH's GPIO27.

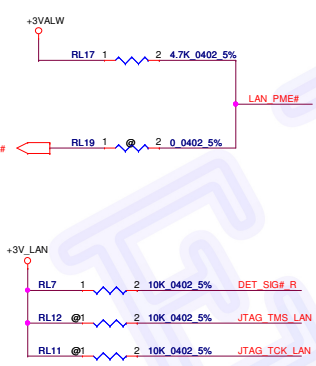
NOTE: LAN\_DISABLE\_N must be connected to PCH's GPIO12/LAN\_PHY\_PWR\_CTRL. This GPIO12 pin must be set as "LAN\_PHY\_PC" function through FITC tool.

Connect RBIAS through a 3.01 kΩ 1% pull-down resistor to ground and then place it no more than one half inch (0.5") away from the PHY.

\*IMPORTANT NOTE: LAN\_PWR\_EN Controls PHY Power

NOTE: Total requirement Cout>=20uF. ESR<50mohm. LAYOUT NOTE: Place LL1, CL7, CL8, CL9, and close to PHY

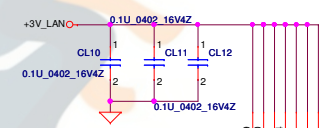
PD	SEL	Function
L	L	Ax to Bx; LEDAx to LEDBx
L	H	Ax to Cx; LEDAx to LEDCx
H	X	Hi-Z



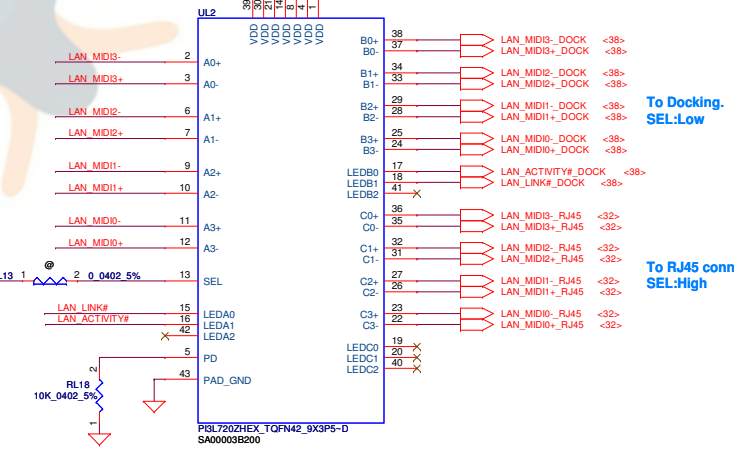
NOTE: Default SMBus Address is 0xC8

#### SMBUS PULL-UP OPTIONS

SMBUS SPEED	RL15 & RL16
1MHz(Default setting)	499ohm
100KHz/400KHz	2.2Kohm



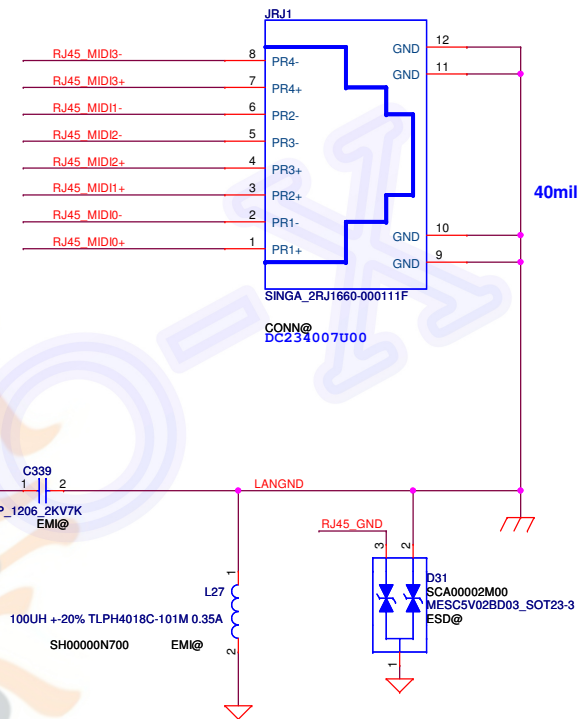
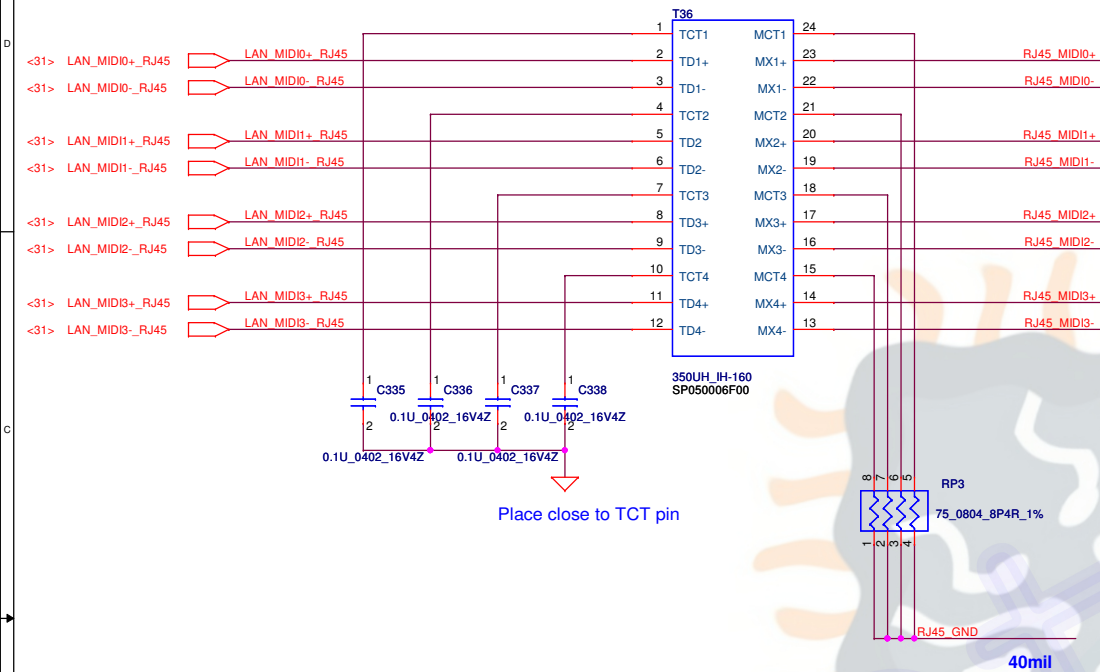
#### LAN Switch



To Docking. SEL:Low


To RJ45 conn SEL:High

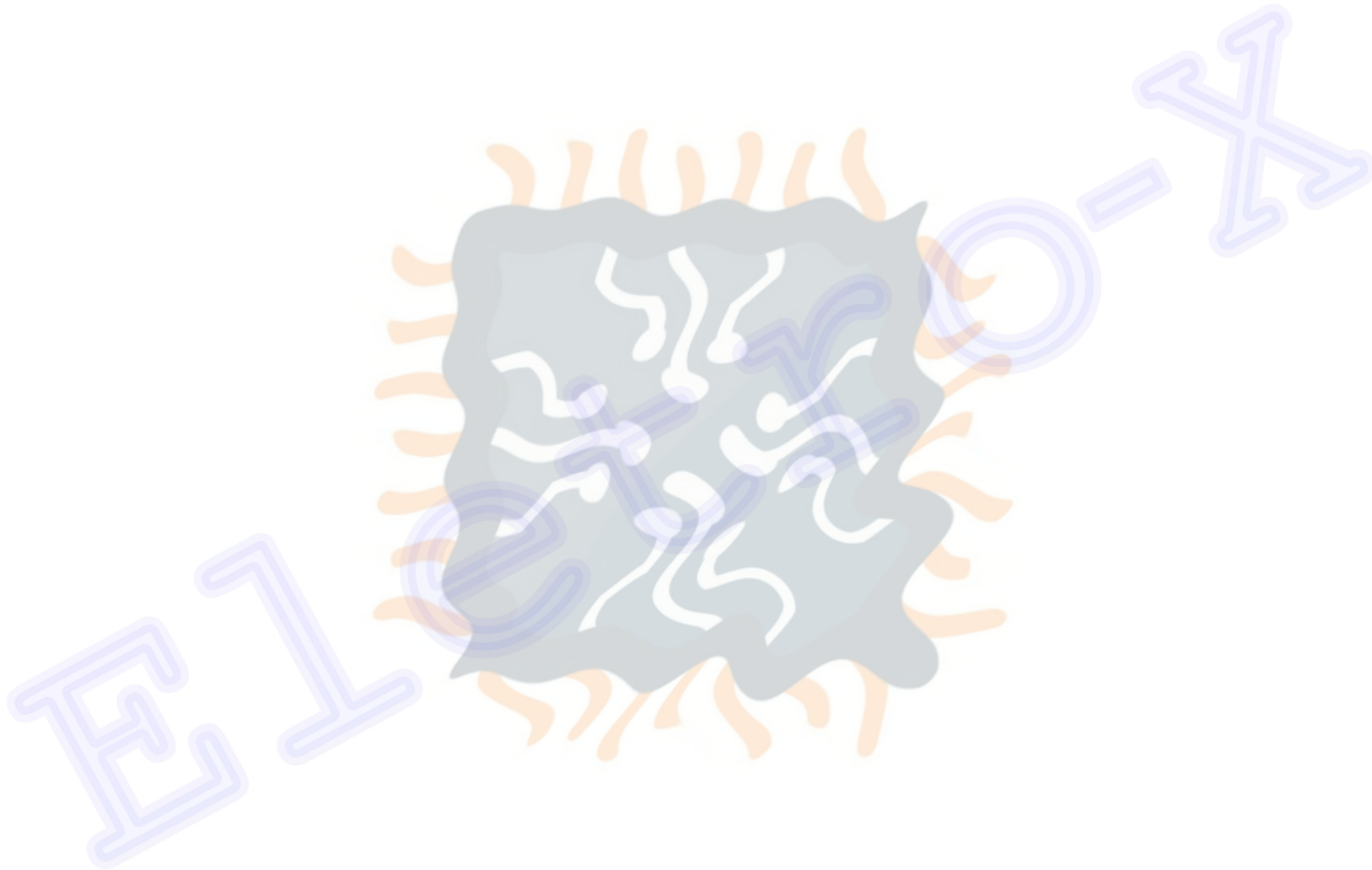
## LAN Connector



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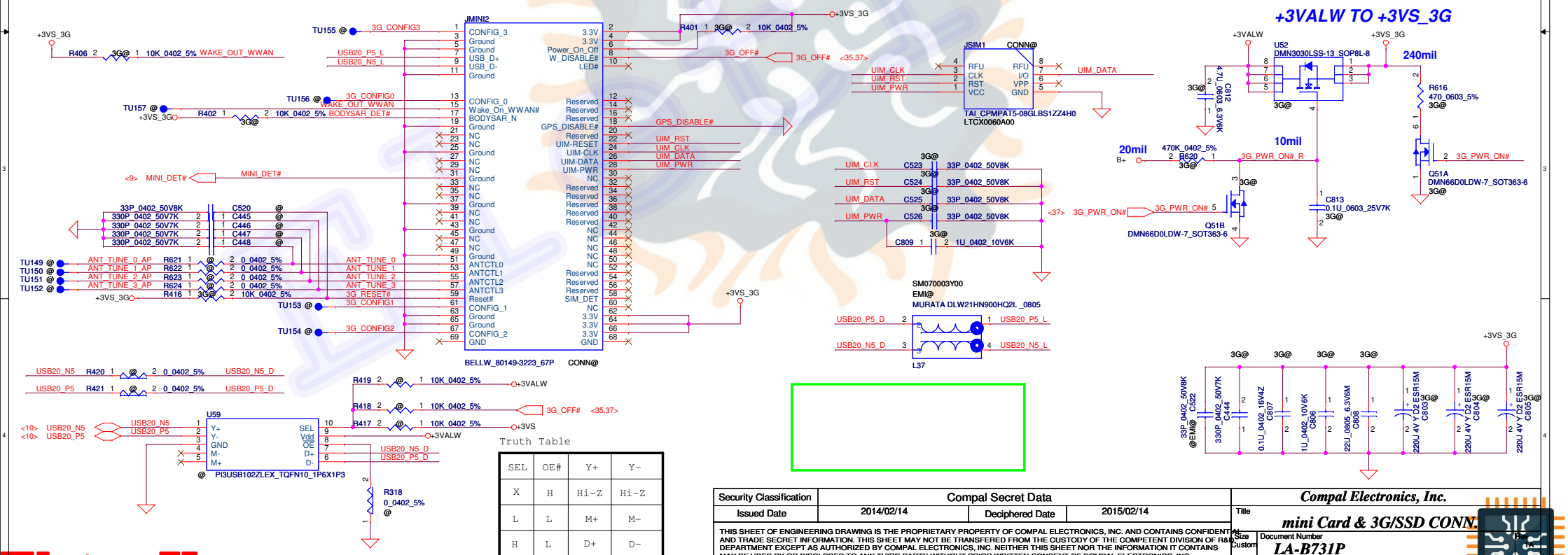
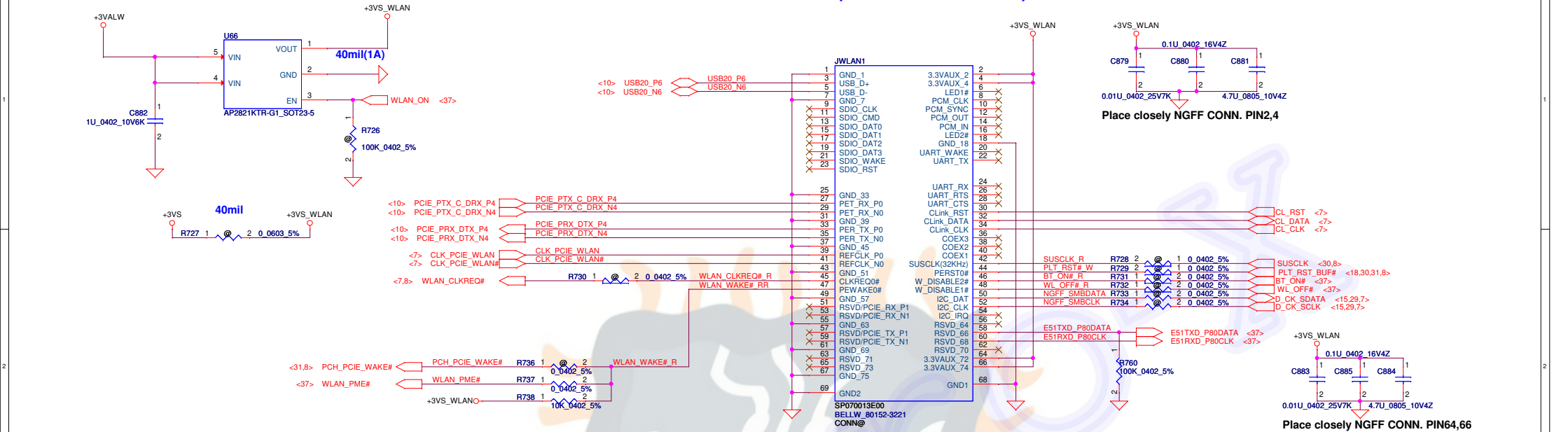


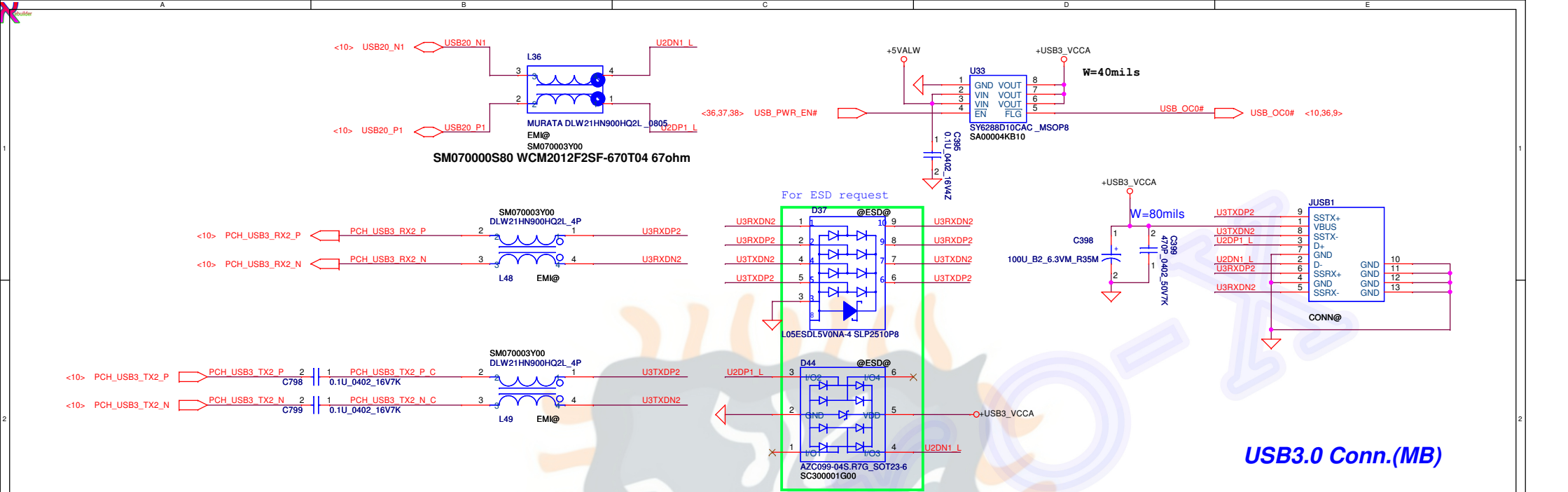


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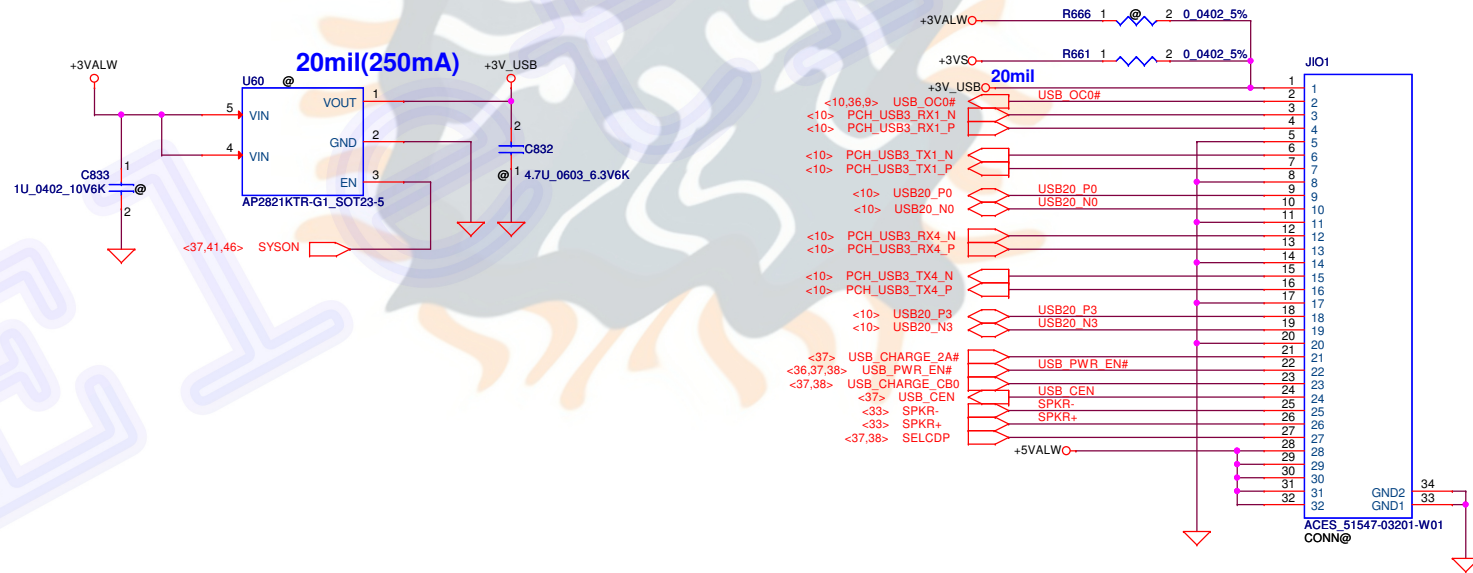


## NGFF(Wireless LAN & BT)



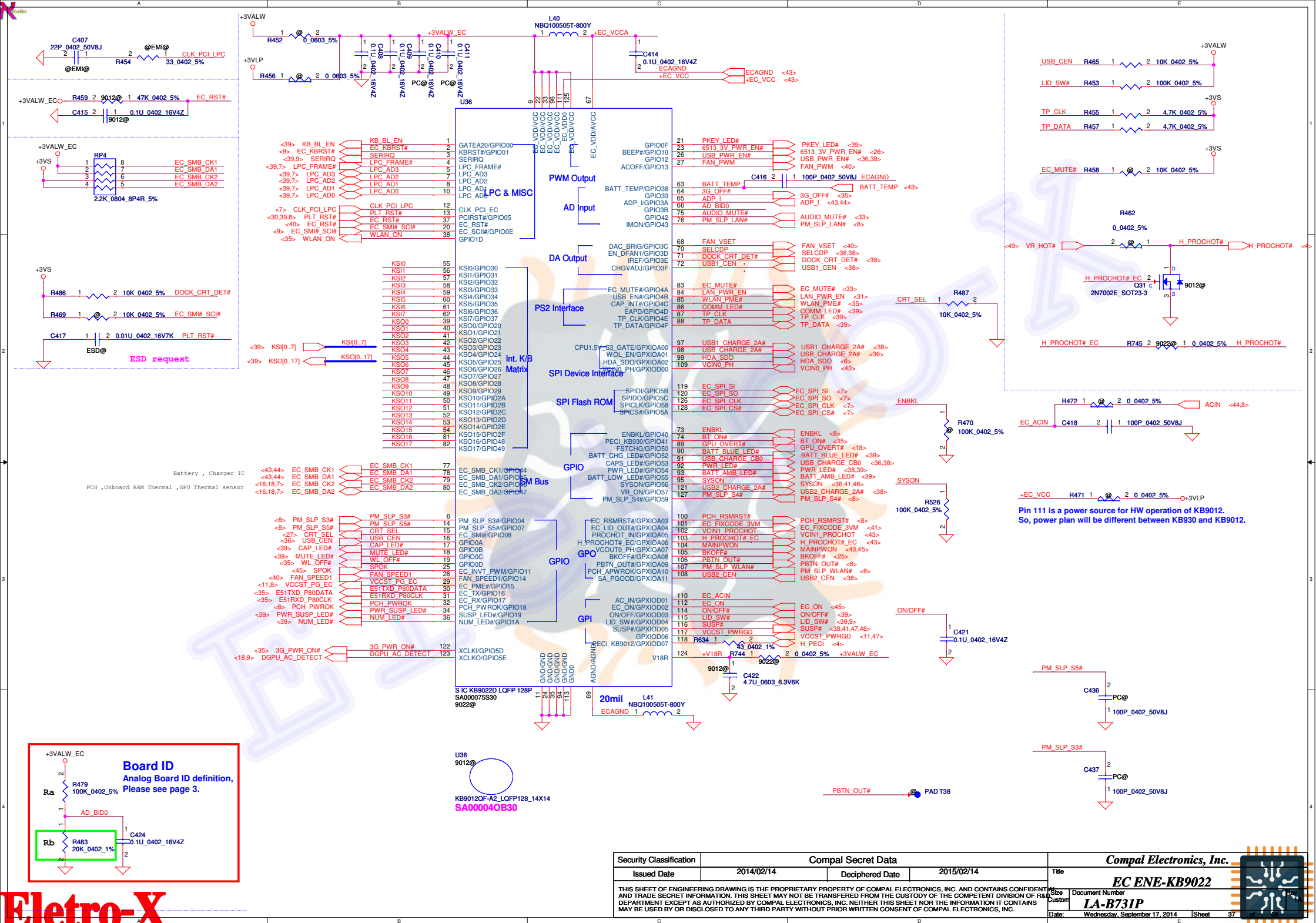


### IO Board Conn(For FFC,FPC)




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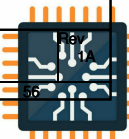






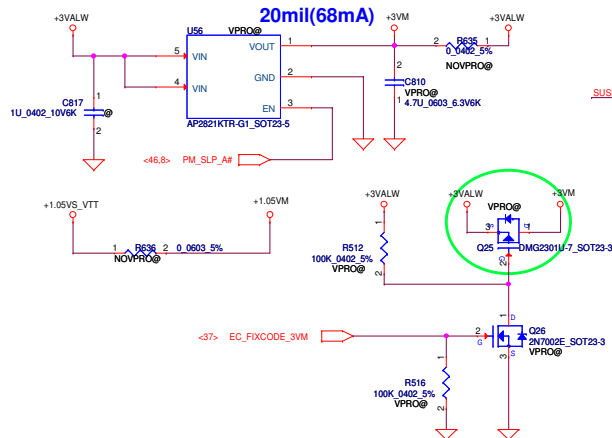


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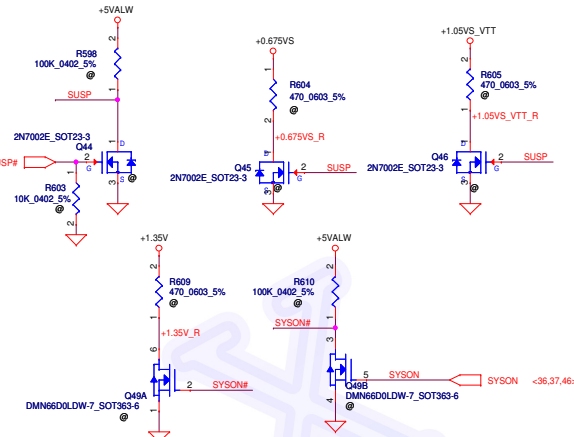
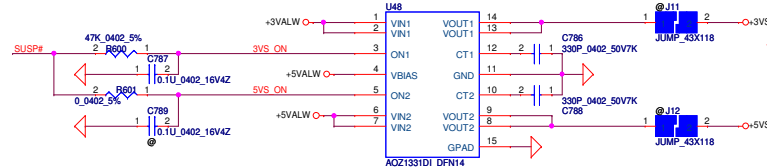




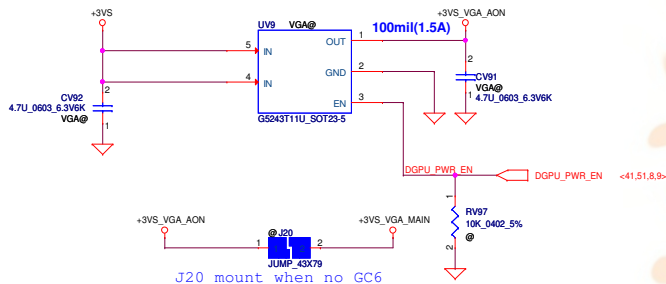
# +3VALW to +3VM for Intel AMT



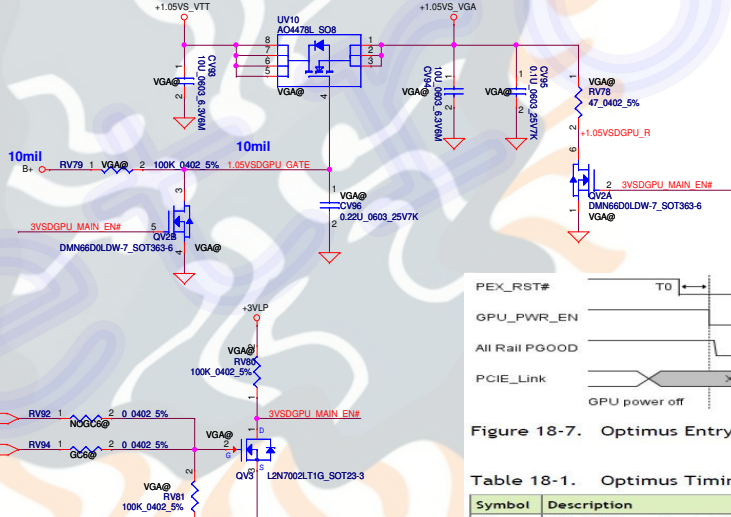
# +3VALW to +3VS +5VALW to +5VS



# +3VS to +3VSDGPU\_AON for GPU



# +1.05VS\_VTT to +1.05VSDGPU



# +3VS to +3VSDGPU\_MAIN for GC6-2.0

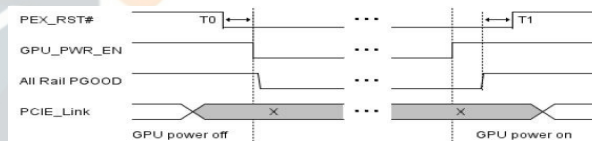
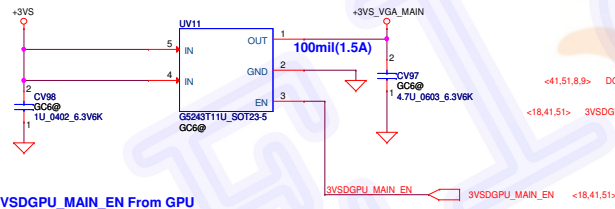
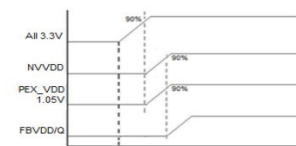


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms



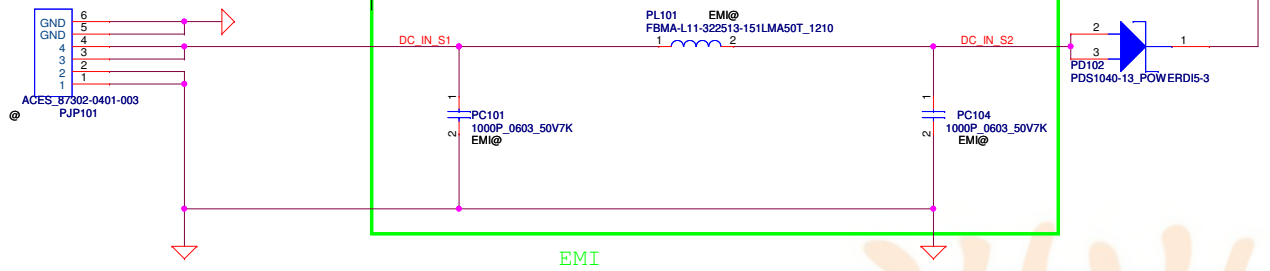
Notes: - All 3.3V includes all rails powered at 3.3V  
- PEX\_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

## Note:

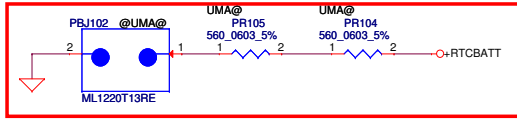
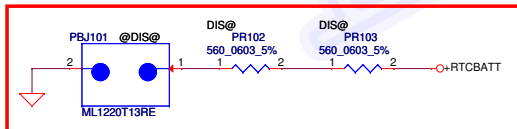
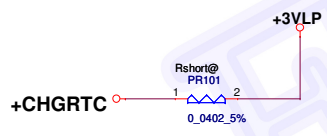
- The ramp time for any rail must be more than 40 μs and is recommended to be less than 2ms.

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				Date:	Wednesday, September 24, 2014	Sheet
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BOM Config

DDR3L	UMA	EMI@
	DIS	EMI@/VGA@/VGAEMI@

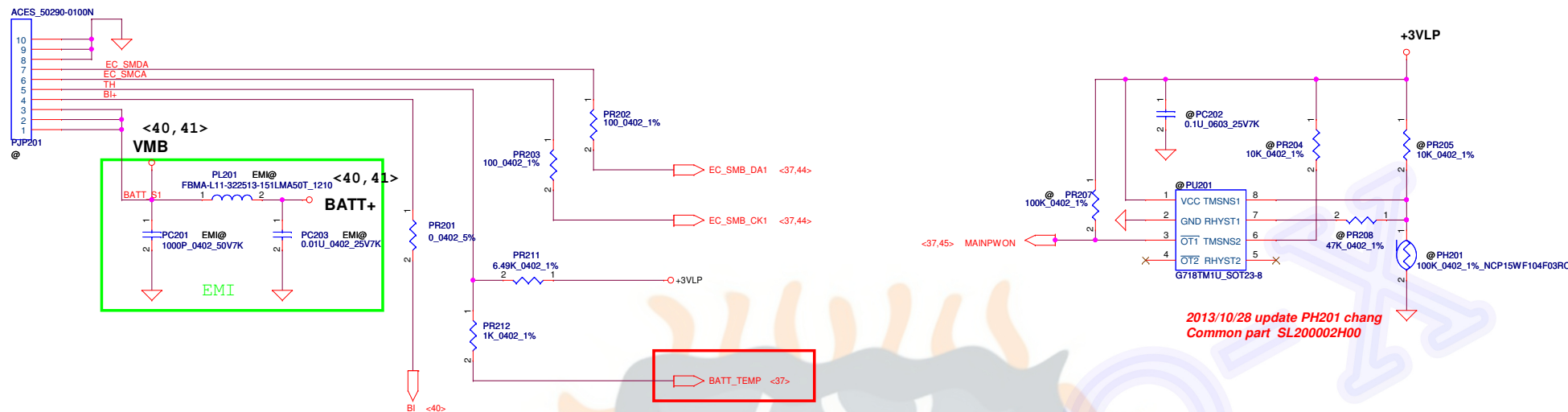


2014/9/17

DIS: RTC at FAN

UMA: RTC at Docking

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								Size		Document Number		V4DA2 LAA131P Schematic	
								Custom		Date		Wednesday, September 17, 2014	
										Sheet		42 of 55	



2013/10/28 update PH201 chang  
Common part SL200002H00

2013/10/14 update

For KB9022 sense 20mΩ	Active	Recovery
40W PR202 10K ohm	52W, 0.54V	40W, 0.42V
65W PR202 22.6K ohm	84.5W, 0.54V	65W, 0.42V

For 65W adapter==>action 84.5W, recovery 65W

65W:

Iada=0~3.42A (65W/19v=3.42A)

ADP\_I=20\*Iada\*Rsense

=20\*3.42\*0.02=1.368V

VCIN1\_PROCHOT=1.368\*10/(10+22.6)=0.42V

84.5W:

Iada=0~4.447A (84.5W/19v=4.447A)

ADP\_I=20\*Iada\*Rsense

=20\*4.447\*0.02=1.788V

VCIN1\_PROCHOT=1.788\*10/(10+22.6)=0.55V

CPU thermal protection at 92 degree C

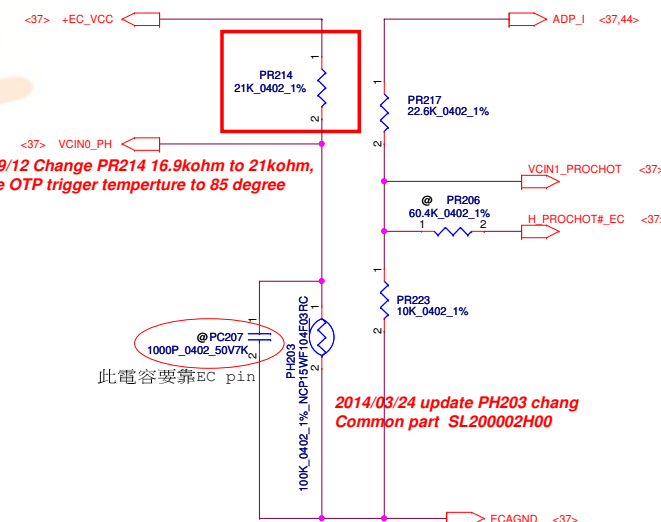
PH203 under CPU botten side :

(92 degree = 7.3K ohm) => VCIN0\_PH = 1V

(56 degree = 26.11k ohm) => VCIN0\_PH = 2V

3.3\*7.3/(7.3+16.9)=1

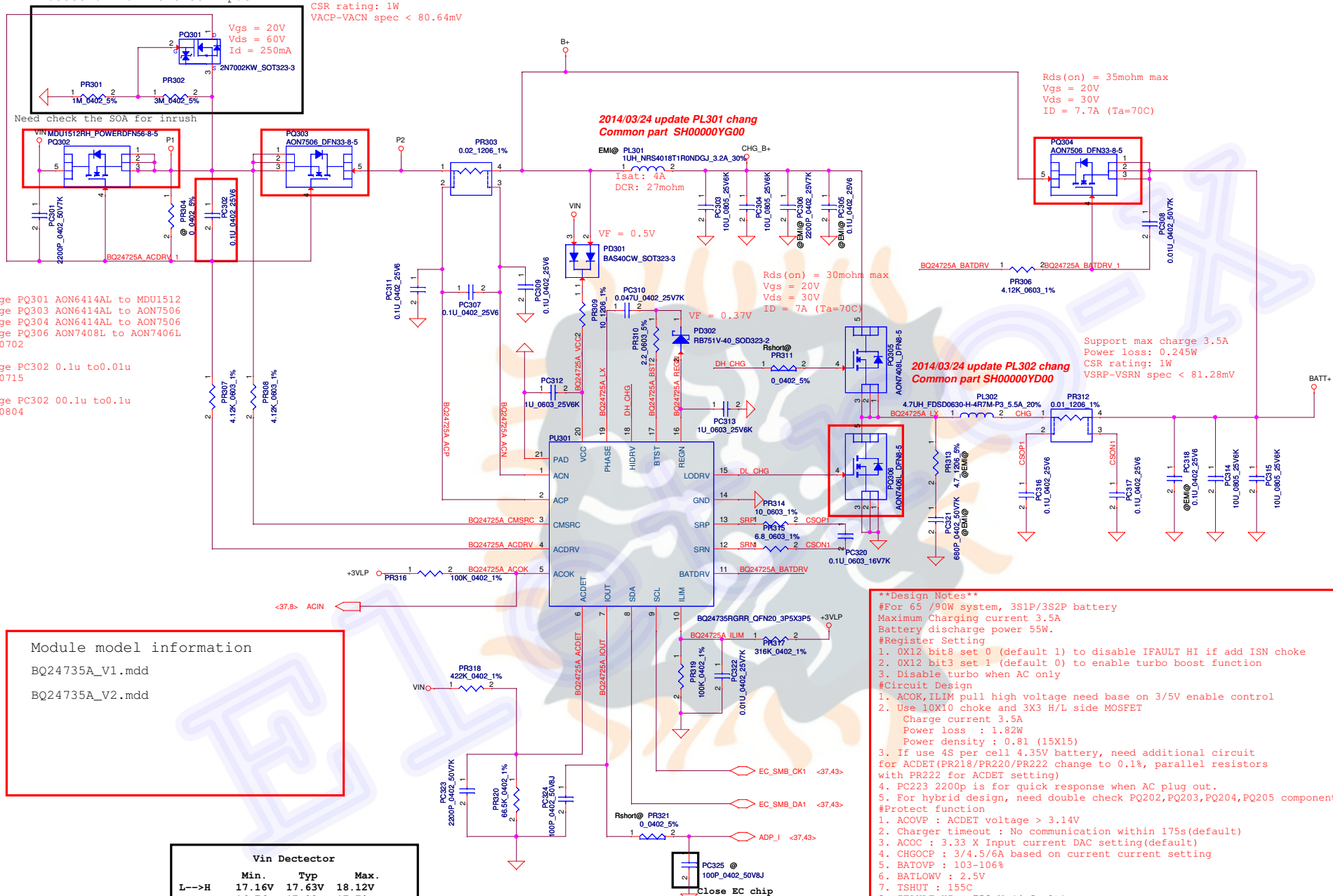
3.3\*26.11/(26.11+16.9)=2



2014/09/12 Change PR214 16.9kohm to 21kohm,  
change OTP trigger temperture to 85 degree

2014/03/24 update PH203 chang  
Common part SL200002H00

max Power loss 0.22W for 90W;0.12W for 65W system  
CSR rating: 1W  
VACP-VACN spec < 80.64mV



## Module model information

BQ24735A\_V1.mdd

B024735A V2.mdd

	Vin Dectector		
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20\*ILIM\*Rsr  
 ILIM =  $3.3 \times 100 / (100 + 107) / 20 / 0.02$   
       = 3.986 A

**\*\*Design Notes\*\***

```
##Design Notes##
#For 65 /90W system, 3S1P/3S2P battery
```

Maximum Charging current 3.5A

Battery discharge power 55W.

## #Register Setting

1. 0X12 bit8 set 0 (default 1) to disable IFault HI if add ISN choke

2. 0X12 bit3 set 1 (default 0) to enable turbo boost function

3. Disable turbo when AC only

## #Circuit Design

1. ACOK, ILIM pull high voltage need base on 3/5V enable control

2. Use 10X10 choke and 3

Charge current 3.5A

Power loss : 1.82W

Power density : 0.81 (15X15)

3. If use 4S per cell 4.35V battery, need additional circuit

for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors

for NODE1 (PR210, PR220, PR222 change to 0.110, parallel resistors with PR222 for ACDET setting)

4. PC223 2200p is for quick response when AC plug out.

5. For hybrid design, need double check PQ202,PQ203,PQ204,PQ20

```
#Protect function
```

```
1. ACOVP : ACDET voltage > 3.14V
```

1. ACVR : ACER voltage > 5.14V
2. Charger timeout : No communication within 175s(default)

3. ACOC : 3.33 X Input current DAC setting(default)

4. CHGOCP : 3/4.5/6A

5. BATOVIP : 103-1

6. BATLOWV : 2.5V

7. TSHUT : 155C

8. IFAULT HI : 750mV (default)

9. IFAULT LOW : 110mV (default)

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				Date	Wednesday, September 17, 2014		Sheet





## SY8208B\_V1.mdd

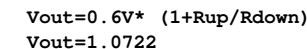
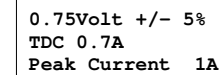


## SY8208C\_V1.mdd

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<h1 style="text-align: center;">Compal Electronics, Inc.</h1>									
Title		3VALW/5VALW							
Part Number	Document Number		V4DA2 LAA131P Schematic					Rev. 001	
Size	Custom		Date	Wednesday, September 17, 2014		Sheet	45	of	55

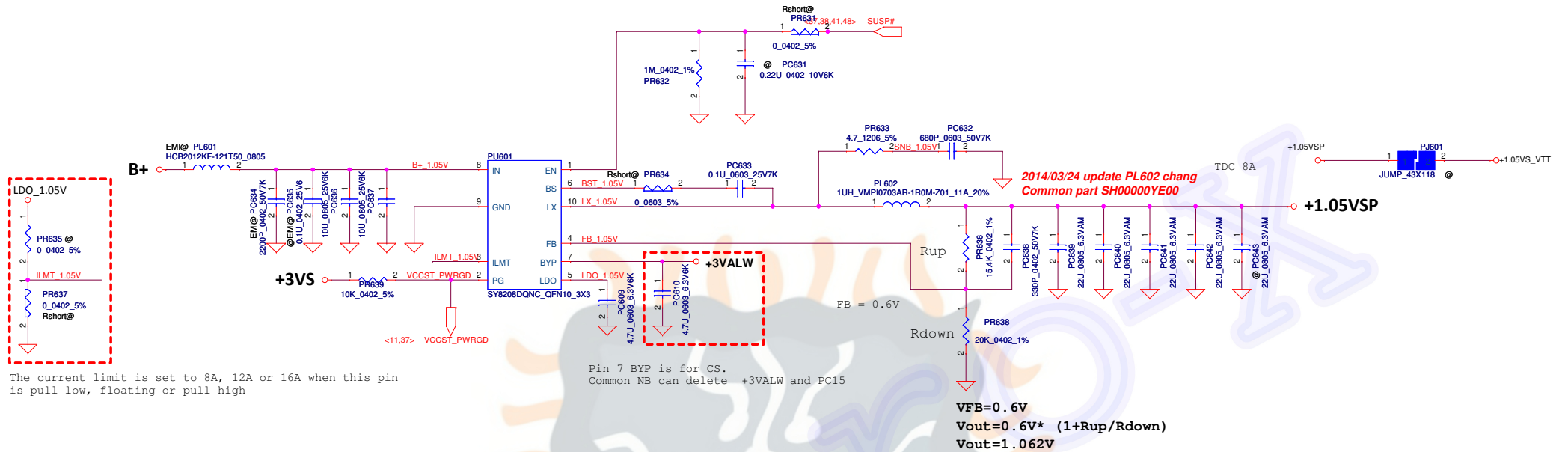




STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

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Issued Date	2012/06/19	Deciphered Date	2012/07/31	Title	
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Size	Document Number				
Custom	V4DA2 LAA131P Schematic				
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EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



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				Customer	V4DA2 LAA131P Schematic
				Date	Wednesday, September 17, 2014
				Sheet	47 of 55
				Rev	0.1



TPS51212\_V1.mdd for Single layer  
TPS51212\_V2.mdd for Dual layer

Pin 7 BYP is for CS.  
Common NB can delete +3VALW and PC15

2014/03/24 update PL702 chang  
Common part SH00000YE00

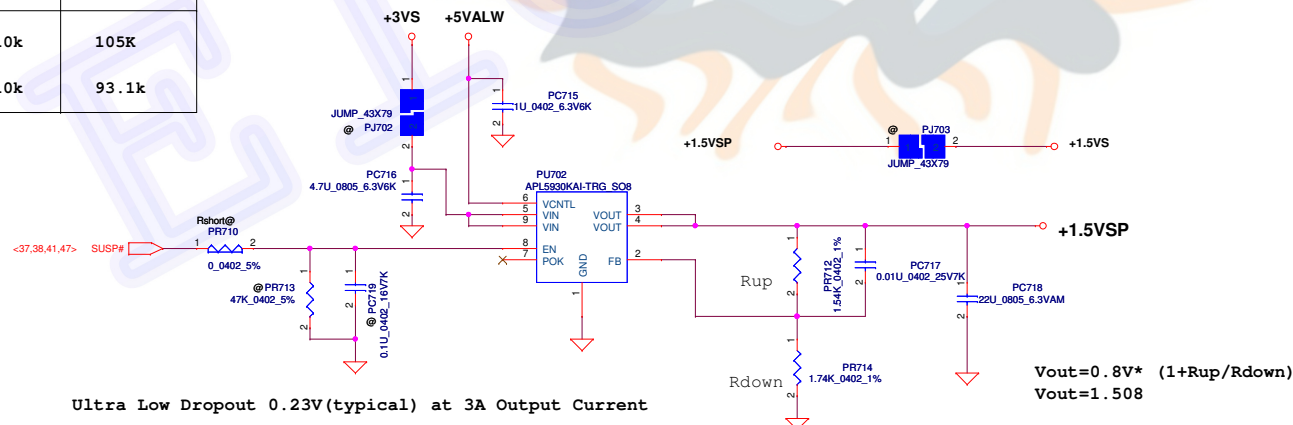
VFB=0.6V  
Vout=0.6V\* (1+Rup/Rdown)  
Vout=1.522V

Switching Frequency: 290kHz  
I<sub>max</sub>=8A  
OCP~10.5A  
OVP: 120%~130%  
VFB=0.704V, V<sub>out</sub>=1.207V

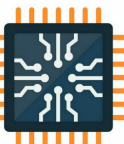
Switching Frequency: 290kHz  
 $I_{max}=5.4A$   
 $I_{peak}=6.5A$   
 $I_{ocp}=7.8A$   
 OVP: 120%-130%  
 $V_{FB}=0.704V$ ,  $V_{out}=1.055V$

MOSFET: 3x3 DFN  
H/S Rds (on): 27mohm(Typ), 34mohm(Max)  
L/S Rds (on): 22mohm(Typ), 13.5mohm(Max)  
  
Choke: 7x7x3  
Rdc=15.5mohm +/-15%  
  
Switching Frequency: 290kHz  
Ipeak=10A  
Delta I = 2.16A  
Iocp=12.14~16.67A  
OVP: 120%~130%  
VFB=0.704V, Vout=1.51V

Vout	PR1007	PR1008	PR1003
+1.5V	11.5k	10k	
+1.35V	9.31k	10k	
+1.2V	7.15K	10k	105K
+1.05V	4.99k	10k	93.1k



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				Date:	Wednesday, September 17, 2014	Sheet 48 of 55





Module model information:  
ISL95813 (for 15W & 28W CPU)

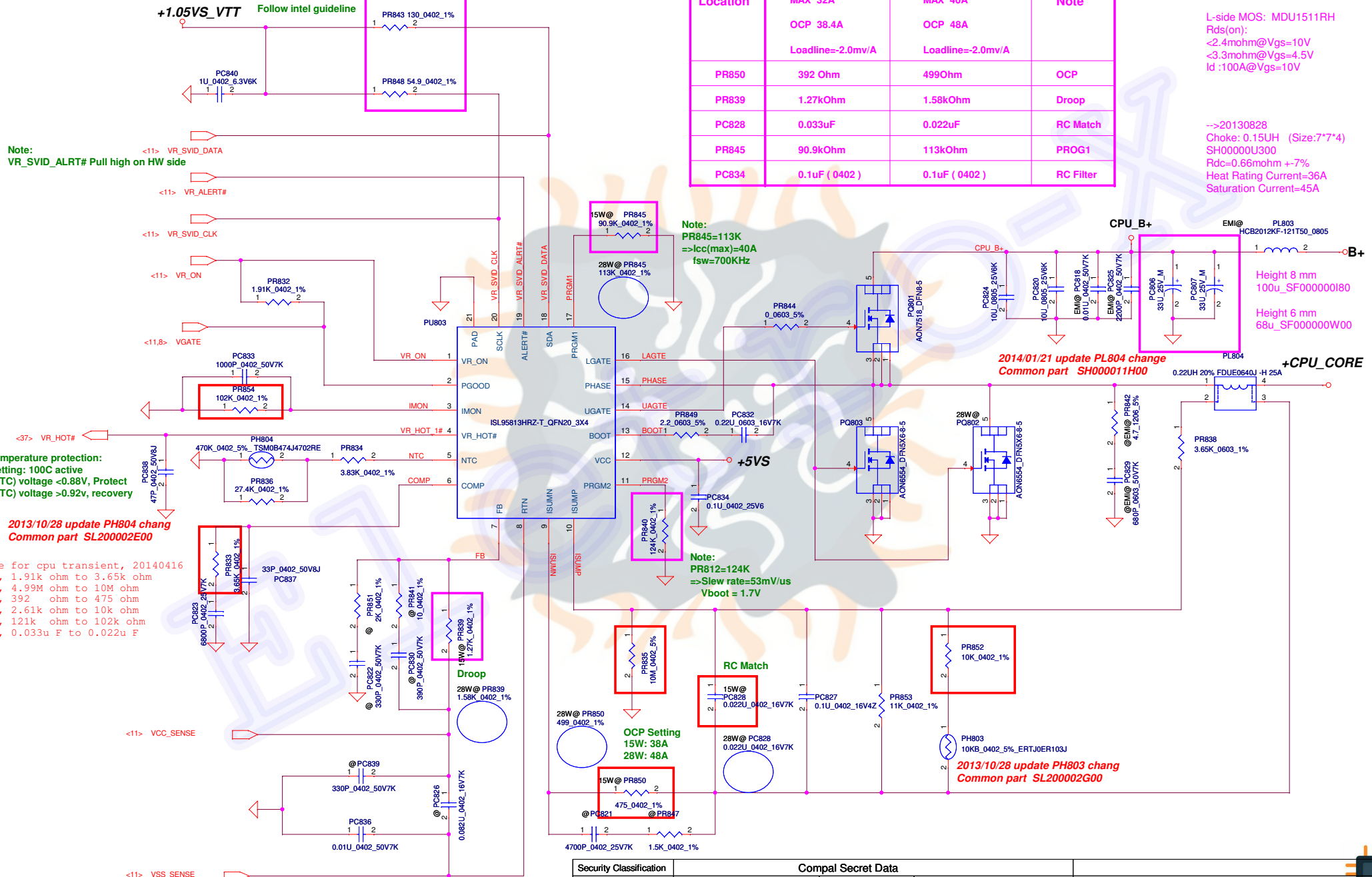
Base on BDW PDDG Rev\_0\_73

Location	15W	28W	Note
	TDC 14A	TDC 19A	
	MAX 32A	MAX 40A	
	OCF 38.4A	OCF 48A	
	Loadline=-2.0mv/A	Loadline=-2.0mv/A	
PR850	392 Ohm	499Ohm	OCF
PR839	1.27kOhm	1.58kOhm	Droop
PC828	0.033uF	0.022uF	RC Match
PR845	90.9kOhm	113kOhm	PROG1
PC834	0.1uF ( 0402 )	0.1uF ( 0402 )	RC Filter

H-side MOS: MDV1525URH  
Rds(on):  
<10.1mohm@Vgs=10V  
<14.0mohm@Vgs=4.5V  
Id :24A@Vgs=10V

L-side MOS: MDU1511RH  
Rds(on):  
<2.4mohm@Vgs=10V  
<3.3mohm@Vgs=4.5V  
Id :100A@Vgs=10V

-->20130828  
Choke: 0.15UH (Size:7\*7\*4)  
SH00000U300  
Rdc=0.66mohm +-7%  
Heat Rating Current=36A  
Saturation Current=45A



Module model information:  
RT8813A\_V1A for IC module  
RT8813A\_V1B for SW module

Vboot=Vvref\*(Rref2/(Rref1+Rref2+Rboot))  
Rt=Rrefadj/(Rboot+Rref2)  
Vmin=Vvref\*(Rref2/(Rref2+Rboot))\*[Rt/(Rref1+Rt)]  
Vmax=Vvref\*(Rref2/((Rref1/Rrefadj)+Rboot+Rref2))  
Vout=Vmin+N\*Vstep  
Vstep=(Vmax-Vmin)/Nmax

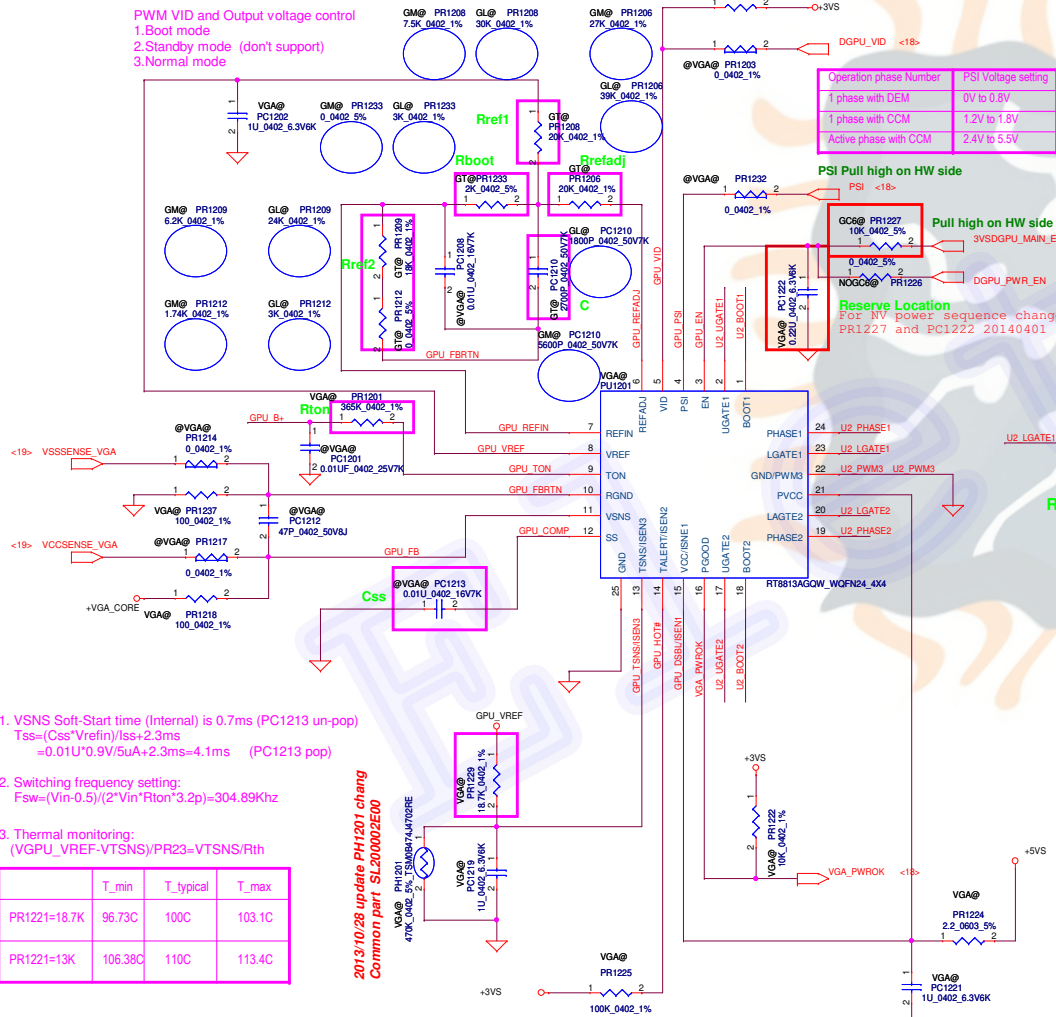
PWM-VID Spec and component Values

PWM-VID Spec	Config B	Config C	Config D
Vmin	0.6V	0.65V	0.9V
Vmax	1.2V	1.15V	1.15V
Vboot	0.9V	0.9V	1.028V
Voltage step	6.25mV	25mV	12.5mV
N of Voltage level	96	20	20
Rrefadj	PR1206 20K	39K	27K
Rref1	PR1208 20K	30K	7.5K
Rboot	PR1233 2K	3K	0
Rref2=PR1209 +PR1212	PR1209 18K	24K	6.2K
	PR1212 0	3K	1.74K
C	PC1210 2.7nf	1.8nf	5.6nf

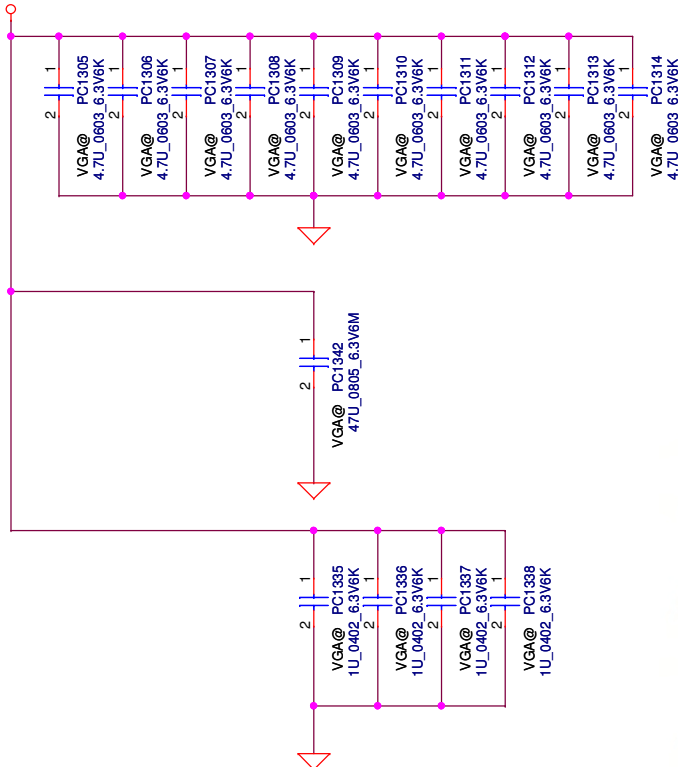
Current Limit threshold setting  
Rocset= (Ivalley \* Rds(on) + 40 mV) / 10uA  
I\_ripple=(19-0.9)\*0.9/  
(304.89KHz\*0.36u\*19)=7.811A  
OCP=54A/2=27A per phase  
Ivalley=27A\*7.811A/2=23.1A  
H-side MOS:AON6552  
Rds(on):  
5.6mohm@Vgs=10V  
6.7mohm@Vgs=4.5V  
Id :20A@Ta=25 degC  
L-side MOS:AON6554  
Rds(on):  
3.2mohm@Vgs=10V  
3~3.8mohm@Vgs=4.5V  
Id :85A@Ta=25 degC  
Choke: 0.22uH (Size:7\*7\*4)  
Rdc=0.97mohm +5%  
Heat Rating Current=34A  
Saturation Current=25A  
C=3\*330uF (9mohm)=990uF  
Vripple=tripple\*ESR(min)=7.811A\*3mohm=23.4mV

Different VGA Chip (different EDP-Peak Current) need select different solution

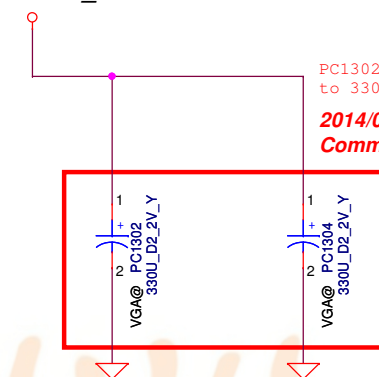
VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config C
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@



# **+VGA\_CORE** Under VGA Core



# **+VGA\_CORE**

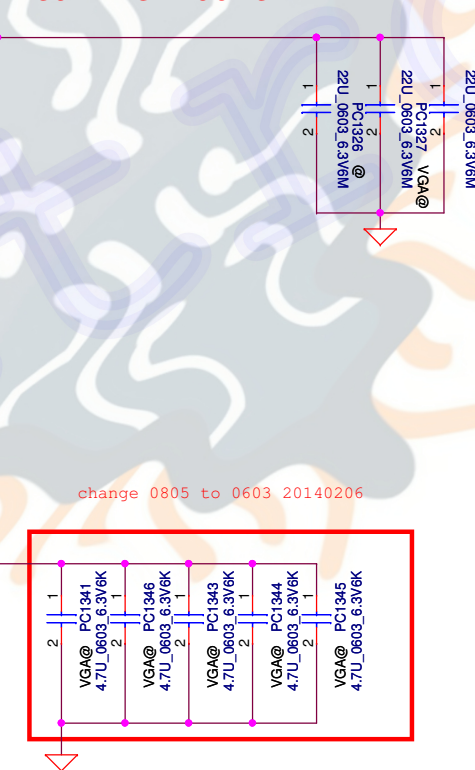


PC1302 and PC1304 change 560U to 330U 20140124

2014/08/18 update PC1302 & PC1304 chang Common part SGA00009S00

# **+VGA\_CORE**

## Near VGA Core



change 0805 to 0603 20140206

N15x 2013/12/10  
Under  
4.7uF\_0603\_10pcs  
1uF\_0402\_4pcs  
Near  
47uF\_0805\_1pcs  
22uF\_0603\_1pcs (2PCS unpop)  
4.7uF\_0805\_5pcs

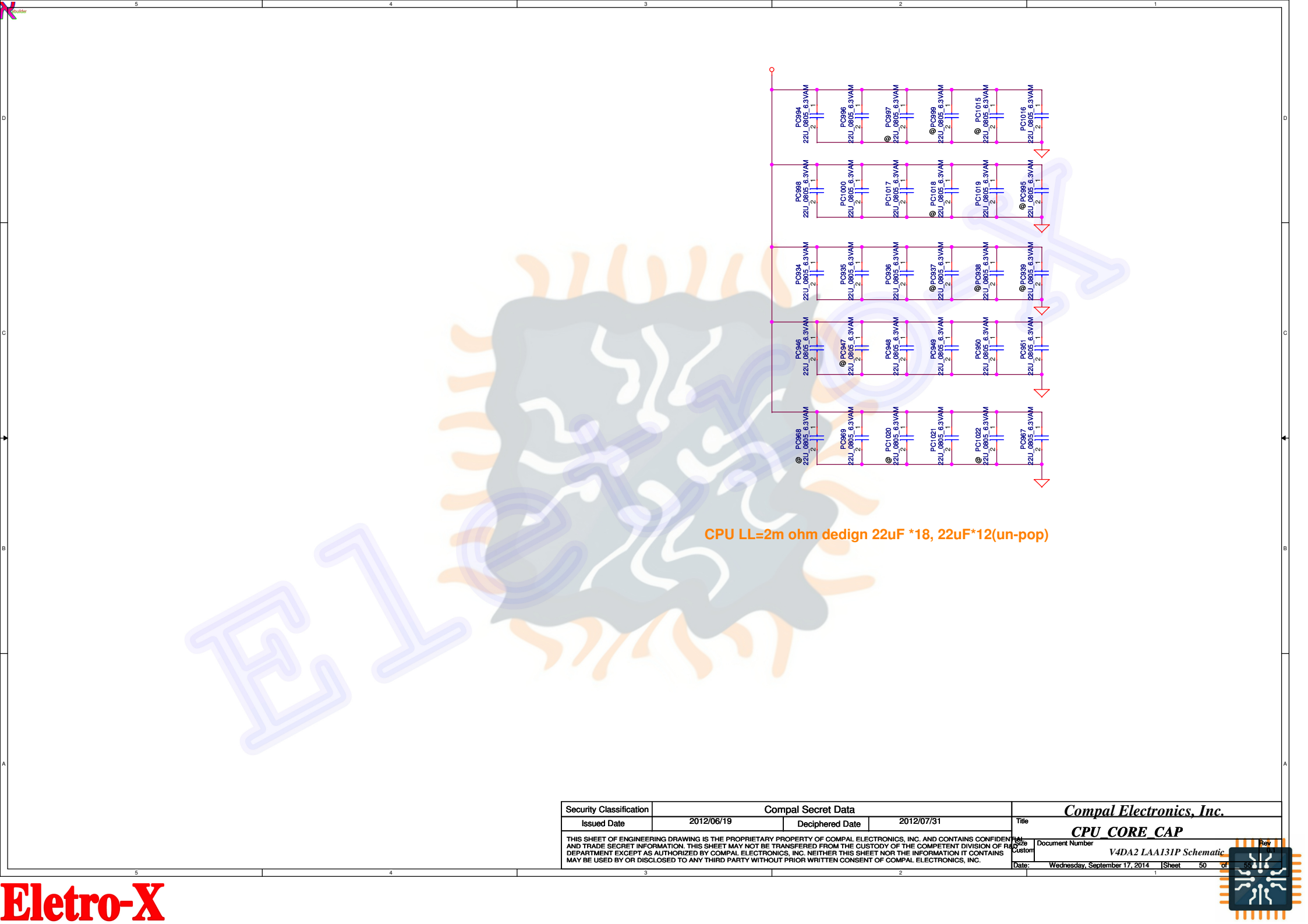
N15x2013/10/17  
Under  
4.7uF\_0603\_15pcs  
1uF\_0402\_8pcs  
Near  
47uF\_0805\_0pcs  
22uF\_0603\_9pcs (2PCS unpop)  
4.7uF\_0805\_5pcs

N15x2013/10/07  
Under  
4.7uF\_0603\_15pcs  
1uF\_0402\_8pcs  
Near  
47uF\_0805\_0pcs  
22uF\_0805\_9pcs (2PCS unpop)  
4.7uF\_0805\_5pcs

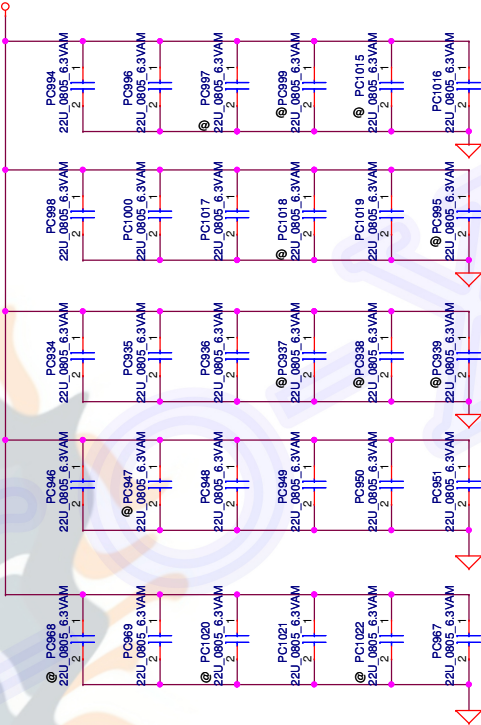
N15x2013/10/02  
Under  
4.7uF\_0603\_15pcs  
1uF\_0402\_8pcs  
Near  
47uF\_0805\_0pcs  
22uF\_0805\_14pcs  
4.7uF\_0805\_5pcs

N14x  
Under  
4.7uF\_0603\_10pcs  
0.1uF\_0402\_4pcs  
Near  
47uF\_0805\_1pcs  
22uF\_0805\_1pcs  
4.7uF\_0805\_5pcs

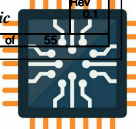
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CPU LL=2m ohm dedign 22uF \*18, 22uF\*12(un-pop)



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## Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Change.	Design Change for common part circuit	0.2	46	Delete PR505 resistor	2014/03/24	DVT
02	Design Change.	Design Change for CPU transient test	0.2	49	Change PR833, 1.91k ohm to 3.65k ohm		
03	Design Change.	Design Change for CPU transient test	0.2	49	Change PR835, 4.99M ohm to 10M ohm		
04	Design Change.	Design Change for CPU transient test	0.2	49	Change PR850, 392 ohm to 475 ohm		
05	Design Change.	Design Change for CPU transient test	0.2	49	Change PR852, 2.61k ohm to 10k ohm		
06	Design Change.	Design Change for CPU transient test	0.2	49	Change PR854, 121k ohm to 102k ohm		
07	Design Change.	Design Change for CPU transient test	0.2	49	Change PC828, 0.033u F to 0.022u F		
08	Design Change.	Design Change for Efficiency test	0.2	47	Change PC639, 47u F to 22u F		
09	Design Change.	Design Change for Efficiency test	0.2	47	Change PC640, 47u F to 22u F		
10	Design Change.	Design Change for Efficiency test	0.2	47	Add PC643 22u F		
11	Design Change.	Design Change for 1.05VMP circuit	0.2	46	Change PR531 100k to 10k for CL_RST1# high > 500us after APWROK high		
12	Design Change.	Design Change for charger circuit	0.2	44	Change PQ302 AON6414AL to MDU1512		
13	Design Change.	Design Change for charger circuit	0.2	44	Change PQ303 AON6414AL to AON7506		
14	Design Change.	Design Change for charger circuit	0.2	44	Change PQ304 AON6414AL to AON7506		
15	Design Change.	Design Change for charger circuit	0.2	44	Change PQ306 AON7408 to AON7406		
16	Design Change.	Design Change for charger circuit	0.2	44	Change PC302 0.1uF to 0.01uF		
17	Design Change.	Design Change for charger circuit	0.2	44	Change PC302 0.01uF to 0.1uF		
18	Design Change.	Design Change for 3VALW 5VALW	0.2	45	Del PR405 4.3k ohm		
19	Design Change.	Design Change for DCIN circuit	0.2	42	Del PQ101, PD103, PD104, PR107, PR109, PC107, PC106, PR108, PR105, PUI01, PC105, PR104, PR109		
20	Design Change.	Design Change for Battery Conn & OTP	0.2	43	Change PR214 16.9kohm to 21kohm, change OTP trigger temperture to 85 degree		

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EVT2-->DVT

- 1.Page 40, Add Fan driver IC
- 2.Page 18, Remove Alert of GPU
- 3.Page 37,Update EC version to D
- 4.Page 28,R633,R665,R667,R668,R669,R671,R630,R631 change to 6.2ohm
- 5.Page 28,L15~L18 change to @EMI@
- 6.Page 31,Add RL18 for second source
- 7.Page 35,Add CLP1 and CLP2 for 3G door
- 8.Page 37,R483 change to 15K for EC ID
- 9.Page 29,remove R746~R749,R757~R759
- 10.Page 11, Add CU157 and CU158 for ESD@
- 11.Page 37,Remove JDB1
- 12.Page 27,Add R762
- 13.Page 4,Update CPU BOM option

DVT-->PVT

- 1.Page 35, remove CLP1 and CLP2
- 2.Page 41,U48 change PN to SA00006U300
- 3.Page 18, GPU thermal SMBUS connect change to EC SMBUS\_2
- 4.Page 18,DGPU\_HOLD\_RST# change to Pull-Low
- 5.QA3 and Q23 and Q25 change PN to SB00000PJ00
- 6.Page 36, D37 and D44 change to @ESD@
- 7.Page 37,EC Board ID, R483 change to 20K
- 8.Page 8, RU161 BOM structure change to UMA@
- 9.Page1,change DAZ number to DAZ18000300
- 10.Page 1,LS-A135P change to LS-B734P (Finger Print)
- 11.Page 29,Create X76PAR@ and X76TI@
- 12.Page 4, Add CPU BOM option
- 13.Page ,C520,C522,C523,C524,C526 form SE068330K80 change to SE071330J80
- 14.Page9 ,RU176 change to mount

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